ANALOG DEVICES

Integrated Digital CCIR-601 YCrCb to PAL/NTSC Video Encoder

Preliminary Technical Information

ADV7177/ADV7178

FEATURES

CCIR-601 YCrCb to PAL/NTSC Video Encoding
NTSC-M/N, PAL-M/N, PAL-B/D/G/H/I
27MHz Oversampled Clocking Rate
32-Bit Direct Digital Synthesiser for Color Sub-Carrier
9-Bit DAC resolution
Multi-standard video output support:
  Composite (CVBS)
  Component S-Video (Y/C)
  Component YUV & RGB
Video Input Data Port supports:
  CCIR-656 4:2:2 8-Bit Parallel Input Format
  4:2:2 16-Bit Parallel Input Format
SMPTE 170M NTSC Compatible Video Output
CCIR-470/CCIR-656 Compatible Video Output
Full Video Output Drive or Low Signal Drive Capability
  -34.7 mA max into 37.5 Ohms (doubly-terminated 75)
  -5 mA min with external buffers
Programmable Simultaneous Composite Video
  and S-VHS Y/C or RGB/YUVVideo Outputs.
Programmable Luma Filters (Low-Pass/Notch)
CCIR-601 and Square Pixel Operation
Programmable VBI (Vertical Blanking Interval)
Programmable Sub-Carrier Frequency and Phase.
Programmable LUMA Delay
Individual ON/OFF Control of Each DAC
Color Signal Control/Burst Signal Control
Interlaced/Non Interlaced Operation
Complete on-chip Video Timing Generator
Programmable Multi-Mode Master/Slave Operation
Macrovision Anti-Taping Rev 7.01 (ADV7178 only)*
8 Color On-Screen Display (ADV7177 only)
Close Captioning support.
13.5 MHz Output Pin for MPEG System Clock
On Board Color Bar Generation
On Board Voltage Reference
Low Power Operational Mode
2 Wire Serial MPU Interface (I^2C Compatible)
Single Supply +5 V or + 3 V Operation
44-Pin PQFP Thermally Enhanced Package

APPLICATIONS

MPEG-1 and MPEG-2 Video, DVD, Digital Satellite/Cable Systems (Set Top Boxes/IRDs), Digital TVs, CD Video/ Karaoke, Video Games, PC Video/Mulimedia

GENERAL DESCRIPTION

The ADV7177/ADV7178 is an integrated Digital Video Encoder that converts Digital CCIR-601 4:2:2 8 or 16-bit Component Video Data into a standard analog baseband television signal compatible with world wide standards. The 4:2:2 YUV Video data is interpolated to two times the pixel rate. The Color-Difference Components (UV) are quadrature modulated using a Sub-Carrier frequency generated by an on-chip 32-Bit digital synthesiser (also running at two times the pixel rate). The two times Pixel Rate sampling allows more accurate generation of the Sub-Carrier because Frequency and Phase Errors are reduced by the higher Sampling Rate. In addition to the Composite output signal, there is the facility to output S-VHS Y/C Video and analog RGB/YUV. The Y/C format is simultaneously available at the Analog Outputs with the Composite Video Signal.
Each Analog Output is capable of driving the full Video-Level (35 mA) signal into an unbuffered, Doubly Terminated 75 Ohm load. With external buffering, the user has the option to scale back the DAC output current to 5 mA min, thereby significantly reducing the power dissipation of the device.
The ADV7177/ADV7178 also supports both a PAL and NTSC square pixel mode in slave mode.
The Output Video Frames are synchronised with the incoming data Timing Reference Codes. Optionally the Encoder accepts (and can generate) HSYNC, VSYNC & FIELD Timing Signals. These timing signals can be adjusted to change pulse width and position while the part is in the master mode. The Encoder requires a single two times pixel rate (27 MHz) Clock for standard operation. This is provided by either a clock or crystal input. Alternatively the Encoder requires a 24.54 MHz Clock for NTSC or 29.5MHz Clock for PAL square pixel mode operation. All internal clocks are generated on-chip. Other features of the ADV7177/ADV7178 include an internal color bar generator, lower power mode and the ability to switch the DACs on and off individually. The ADV7177(only) provides an 8 color look up table for overlay on the video output. The ADV7178 swaps the OSD for Macrovision's* anticopy algorithm.
The ADV7177/ADV7178 modes are set up over a two wire serial bi-directional port (I^2C Compatible) with 2 slave addresses.
The ADV7177/ADV7178 is protected by US patents numbers 5,343,196 and 5,442,355 and other intellectual property rights.

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* This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. The Macrovision anticopy process is licensed for non-commercial home use only, which is its sole intended use in the device. Please contact sales office for latest Macrovision version available.

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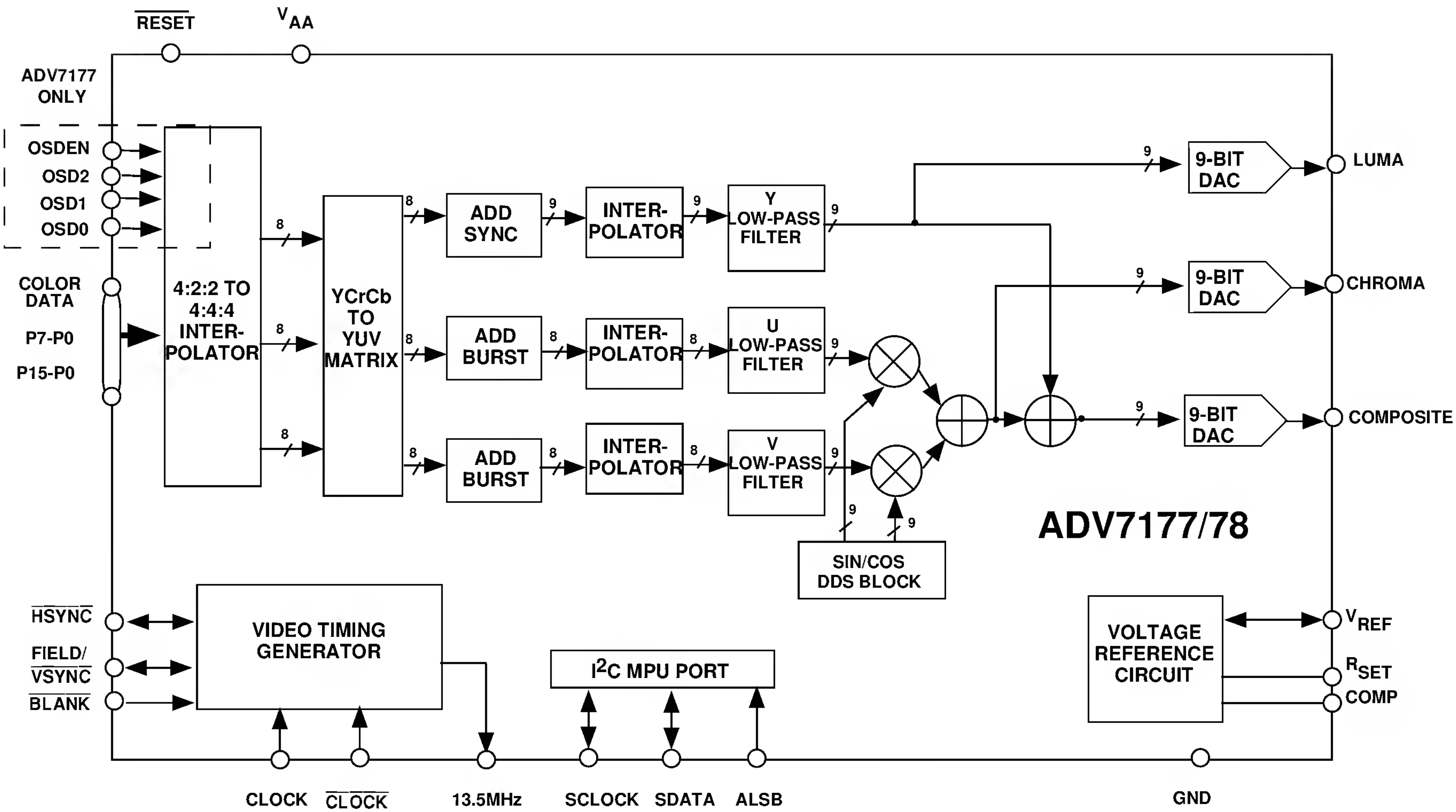
FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

(V_{AA} = + 5V[1], V_{REF} = 1.235 V R_{SET} = 150 Ohms
All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Model Parameter	Conditions[1]	Min	Typ	Max	Units
STATIC PERFORMANCE					
Resolution (each DAC)				9	Bits
Accuracy (each DAC)					
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	µA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 µA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Floating-State Leakage Current				10	µA
Floating-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current[3]		5	34.7	37	mA
Output Current[4]			8		mA
DAC to DAC Matching			2	5	%
Output Compliance, V_{OC}		0		+1.4	V
Output Impedance, R_{OUT}			15		Ký
Output Capacitance, C_{OUT}	I_{OUT} = 0mA			30	pF
VOLTAGE REFERENCE					
Voltage Reference Range, V_{REF}	$I_{VREFOUT}$= 20µA	1.112	1.235	1.359	V
POWER REQUIREMENTS[5]					
V_{AA}		3.0	5	5.25	V
I_{DAC}[6]			140	155	mA
I_{CCT}[7]			110	150	mA
Power Supply Rejection Ratio	COMP = 0.1µF		0.02	0.5	% / %

NOTES
[1]±5% for all versions.
[2]Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Full drive into 37.5Ohm load.
[4]Minimum drive with buffered/scaled output load.
[5]Power measurements are taken with Clock Frequency = 27MHz. Max T_J = 110°C.
[6]I_{DAC} is the total current to drive all 4 DACs. Turning off one DAC reduces I_{DAC} correspondingly.
[7]I_{CCT} (Circuit Current) is the continuous current required to drive the device.
[8] Guaranteed by characterisation.
[9] These specifications are for the low pass filter only. For the other internal filters please see Figure 3.
Specifications subject to change without notice.

DYNAMIC-SPECIFICATIONS[1]

Model Parameter	Conditions[1]	Min	Typ	Max	Units
Filter Characteristics					
Luma Bandwidth[9] (Low Pass Filter)	NTSC Mode				
Stop Band Cutoff	>50dB Attenuation			7.5	MHz
Pass Band Cutoff	< 0.06dB Attenuation			2.3	MHz
Chroma Bandwidth	NTSC Mode				
Stop Band Cutoff	>40dB Attentuation			3.6	MHz
Pass Band Cutoff	<.1dB Attenuation			1.0	MHz
Luma Bandwidth[9] (Low Pass Filter)	PAL MODE				
Stop Band Cutoff	>50dB Attenuation			8.0	MHz
Pass Band Cutoff	< 0.06dB Attenuation			3.4	MHz
Chroma Bandwidth	PAL MODE				
Stop Band Cutoff	>40dB Attentuation			4.0	MHz
Pass Band Cutoff	<.1dB Attenuation			1.3	MHz
Differential Gain			0.8		%
Differential Phase			0.8		°
Differential Gain	Lower Power Mode		7		%
Differential Phase	Lower Power Mode		2		°
SNR	RMS		60		dB rms
SNR	Peak Periodic		56		dB p-p
Hue Accuracy			1.0		°
Color Saturation Accuracy			1.0		%

AC CHARACTERISTICS[1]

Parameter	Min	Typ	Max	Units	Condition
Chroma Nonlinear Gain		0.6		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		1		±°	NTSC
Chroma Nonlinear Phase		1.7		±°	PAL
Chroma/Luma Intermod		0.2		±%	Referenced to 714 mV (NTSC)
Chroma/Luma Intermod		0.4		±%	Referenced to 700 mV (PAL)
Chroma/Luma Gain Ineq		0.6		±%	
Chroma/Luma Delay Ineq		1		ns	
Luminance Nonlinearity		0.8		±%	
Chroma AM Noise		60		dB	
Chroma PM Noise		59		dB	

TIMING–SPECIFICATIONS[1]

Parameter	Min	Typ	Max	Units	Condition
MPU PORT[1]					
SCLOCK Frequency	0		100	KHz	
SCLOCK High Pulse Width, t_1	4.0			µs	
SCLOCK Low Pulse Width, t_2	4.7			µs	
Hold Time (Start Condition), t_3	4.0			µs	After this period the 1st clock pulse is generated
Setup Time (Start Condition), t_4	4.7			µs	Relevent for repeated Start Condition
Data Setup Time, t_5	250			ns	
SDATA, SCLOCK Rise Time, t_6			1	µs	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	4.7			µs	
ANALOG OUTPUTS[1,5]					
Analog Output Delay		5		ns	
DAC Analog Output Skew		0		ns	
CLOCK CONTROL AND PIXEL PORT[6]					
F_{CLOCK}	24.52	27	29.5	MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}	3.5			ns	
Data Hold Time t_{12}	1			ns	
Control Setup Time t_{11}	4			ns	
Control Hold Time t_{12}	2			ns	
Digital Output Access Time t_{13}			24	ns	
Digital Output Hold Time t_{14}		6		ns	
Pipeline Delay t_{15}		37		Clock cycles	

NOTES ON TIMING CHARACTERISTICS

[1] Guaranteed by characterisation .

[2] TTL input values are 0 to 3 volts, with input rise/fall times - 3 ns, measured between the 10% and 90% points.
Timing reference points at 50% for inputs and outputs.
Analog output load - 10 pF.

[3] ±5% for all versions

[4] Temperature Range (T_{min} to T_{max}) ; 0 to + 70 °C

NOTES ON ANALOG OUTPUTS

[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

NOTES ON PIXEL PORT

[6] Pixel Port consists of the following inputs:

Pixel Inputs:	P15-P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock Input:	CLOCK

Specifications subject to change without notice.

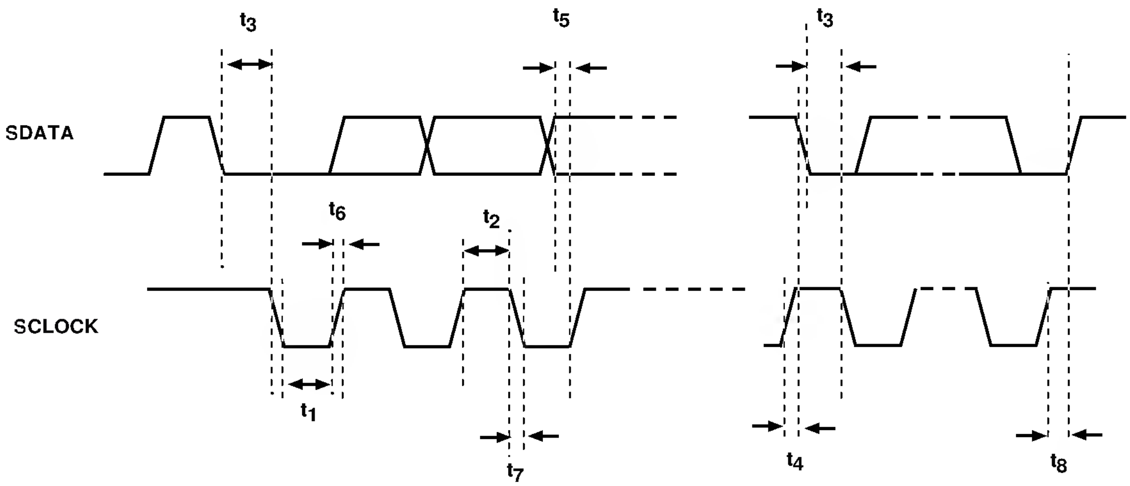


Figure 1. MPU Port Timing Diagram

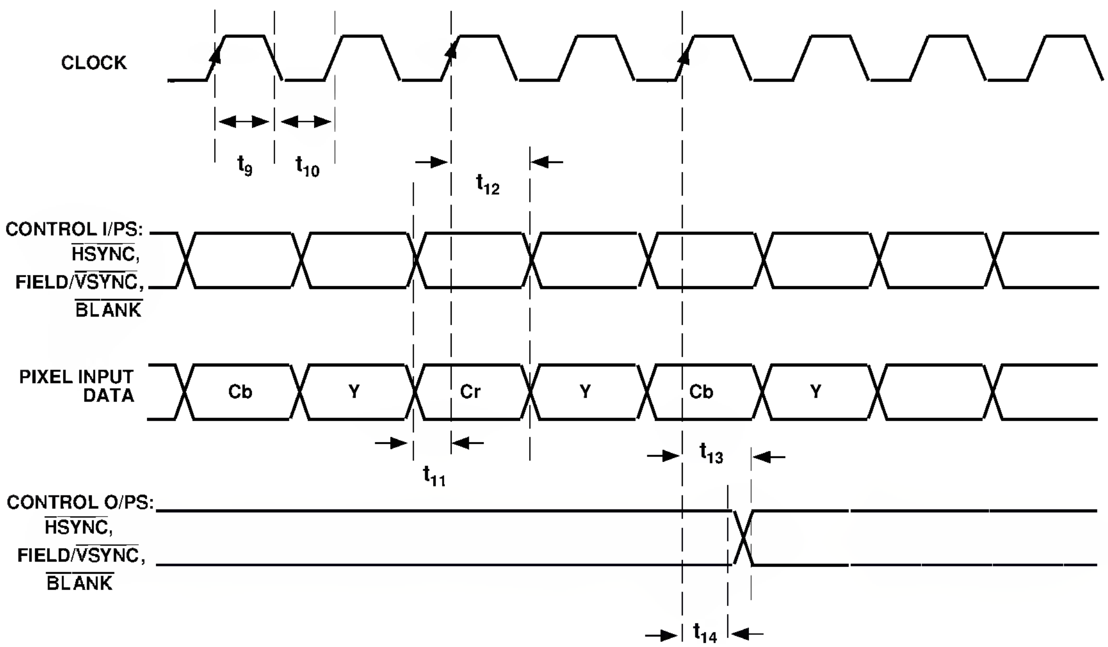


Figure 2. Pixel and Control Data Timing Diagram

ABSOLUTE MAXIMUM RATINGS *

V_{AA} to GND...7V
Voltage on any Digital Input Pin..........GND-0.5V to V_{AA}+0.5V
Storage Temperature (T_S)............................-65°C to +150°C
Junction Temperature(T_J)...+150°C
Lead Temperature (Soldering, 10 secs)......................+260°C
Analog Outputs to GND[1]..........................GND -0.5 to V_{AA}

NOTES

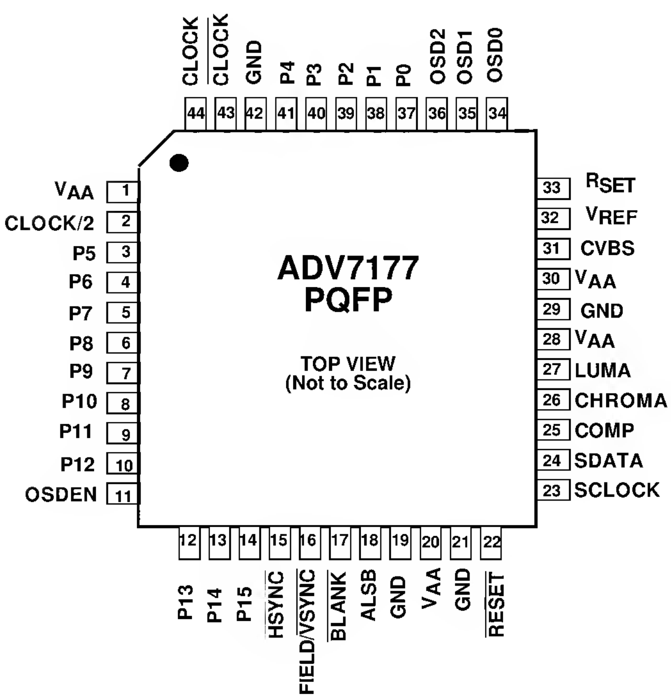
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

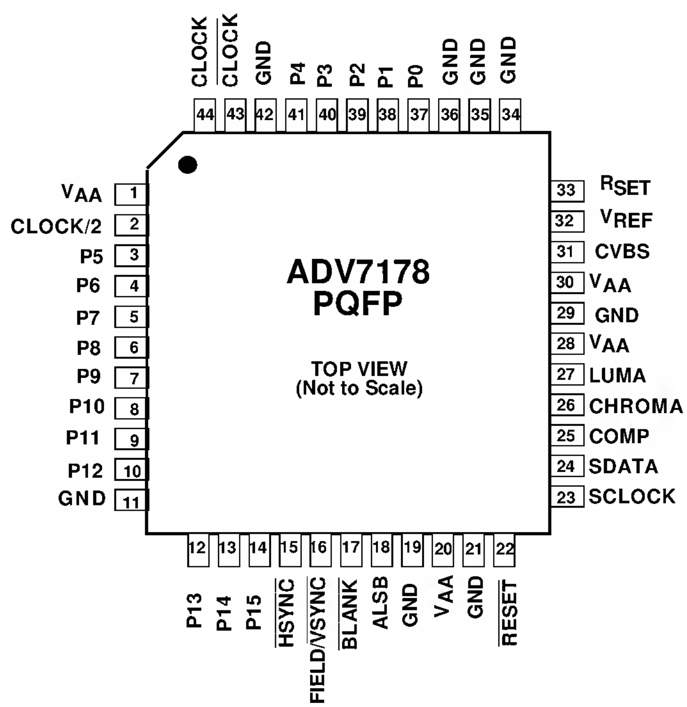
ORDERING GUIDE

Model Option	Temperature Range	Package
ADV7177KS	0°C to 70°C	S-44
ADV7178KS	0°C to 70°C	S-44

ADV7177 PIN CONFIGURATION



ADV7178 PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7177/ADV7178 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

Mnemonic	Input/Output	Function
P15-P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7-P0) or 16-Bit YCrCb Pixel Port (P15-P0). P0 represents the LSB.
CLOCK	I	Crystal Oscillator input. If no crystal is used this pin can be driven by an external TTL Clock source, it requires a stable 27MHz reference Clock for standard operation. Alternatively a 24.52MHz (NTSC) or 29.5MHz (PAL) can be used for square pixel operation.
$\overline{\text{CLOCK}}$	O	Crystal Oscillator output (to crystal). Leave unconnected if no crystal is used.
OSD 0-2	I	On Screen Display Inputs.
OSDEN	I	Enables OSD input data on the video outputs.
CLOCK/2	O	Synchronous Clock output signal. Can be either 27MHz or 13.5MHz, this can be controlled by MR32 and MR33 in Mode Register 3.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 &2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) Sync signals.
FIELD / $\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is logic level "0". This signal is optional.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.2V).
R_{SET}	I	A 150 Ohm resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals.
COMP	O	Compensation Pin. Connect a 0. 1μF Capacitor from COMP to V_{AA}
COMPOSITE	O	PAL/NTSC Composite Video Output. Full-Scale Output is 180IRE (1286mV) for NTSC and 1300mV for PAL.
RED / CHROMA / V	O	RED / S-VHS C / V Analog Output.
GREEN / LUMA / Y	O	GREEN / S-VHS Y / Y Analog Output
BLUE/ CVBS / U	O	BLUE / Composite / U Analog Output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal set up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on chip timing generator and sets the ADV7177/ADV7178 into default mode. This is NTSC operation, Timing Slave Mode 0, 8 Bit Operation, 2 x Composite & S VHS out
V_{AA}	P	+5V Supply.
GND	G	Ground Pin.

DATA PATH DESCRIPTION.

For PAL B,D,G,H,I,M,N and NTSC M,N modes, YCrCb 4:2:2 Data is input via the CCIR-656 Compatible Pixel Port at a 13.5MHz Data Rate. The Pixel Data is de-multiplexed to form three data paths. Y has a range of 16 to 235, Cr and Cb have a range of 128+/-112. The ADV7177/ADV7178 supports PAL (B,D,G,H,I,N,M) and NTSC (with and without Pedestal) standards. The appropriate SYNC, BLANK and Burst levels are added to the YCrCb data. Macrovision Anti-Taping (ADV7178 only) and Close-Captioning levels are also added to Y and the resultant data is interpolated to a rate of 27MHz. The interpolated data is filtered and scaled by three Digital FIR Filters.

The U and V Signals are modulated by the appropriate Sub-Carrier Sine/Cosine Phases and added together to make up the Chrominance Signal. The Luma (Y) signal can be delayed 1-3 Luma Cycles (each cycle is 74ns) with respect to the Chroma Signal. The Luma and Chroma signals are then added together to make up the Composite Video Signal. All edges are slew rate limited.

The YCrCb Data is also used to generate RGB data with appropriate SYNC and BLANK Levels. The RGB data is in sychronisation with the composite video output. Alternatively analog YUV data can be generated instead of RGB.

The four 10-Bit DACs can be used to output :-

(1) 10-Bit Composite Video + 8-Bit RGB Video

(2) 10-Bit Composite Video + 8-Bit YUV Video

(3) Two 10-Bit Composite Video Signals
+ 10-Bit LUMA & CHROMA (Y/C) Signals.

Alternatively, each DAC can be individually powered off if not required.

Video output levels are illustrated in Appendix 3, 4 and 5.

INTERNAL FILTER RESPONSE

The Y Filter supports several different frequency responses including two 4.5/5.0 MHz Low Pass responses and PAL/NTSC Sub-Carrier Notch responses. The U and V Filters have a 0.6/1 .3MHz Low Pass response.

These filter characteristics are illustrated in Figures 3 to 11.

FILTER SELECTION	MR04	MR03	PASS BAND CUTOFF (MHz)	PASSBAND RIPPLE (dB)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)	F_{3dB}
NTSC	0	0	2.3	0.026	7.5	>50	4.2
PAL	0	0	3.4	0.098	8.0	>51.3	5.0
NTSC	0	1	1.0	0.085	3.57	>27.6	2.1
PAL	0	1	1.4	0.107	4.43	>29.3	2.7
NTSC/PAL	1	0	4.0	0.150	8.3	>40	5.65
NTSC	1	1	2.3	0.054	7.5	>54	4.2
PAL	1	1	3.4	0.106	8.0	>50.3	5.0

Figure 3. Luminance Internal Filter Specifications

FILTER SELECTION	PASS BAND CUTOFF (MHz)	PASSBAND RIPPLE (dB)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)	ATTENUATION @ 1.3 MHz (dB)	F_{3dB}
NTSC	1.0	0.085	3.6	>40	0.3	2.05
PAL	1.3	0.04	4.0	>40	0.02	2.45

Figure 4. Chrominance Internal Filter Specifications

Figure 5. NTSC Low Pass Filter

Figure 6. NTSC Notch Filter

Figure 7. PAL Low Pass Filter

Figure 8. PAL Notch Filter

Figure 9. NTSC/PAL Extended Mode Filter

Figure 10. NTSC UV Filter

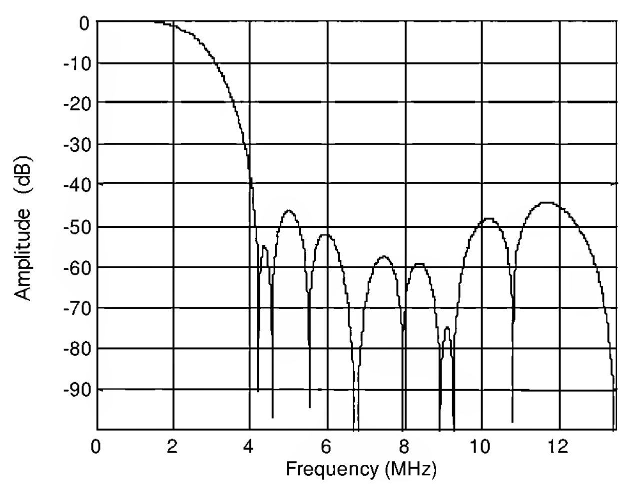


Figure 11. PAL UV Filter

COLOR BAR GENERATION

The ADV7177/ADV7178 can be configured to generate 75% amplitude, 75% saturation (75/7.5/75/7.5) for NTSC or 75% amplitude, 100% saturation (100/0/75/0) for PAL color bars. These are enabled by setting MR17 of Mode Register 1 to logic "1".

SQUARE PIXEL MODE

The ADV7177/ADV7178 can be used to operate in square pixel mode. For NTSC operation an input clock of 24.54MHz is required. Alternatively, for PAL operation, an input clock of 29.5MHz is required. The internal filters scale accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL

The color information can be switched on and off the video output using Bit MR24 of Mode Register 2.

BURST SIGNAL CONTROL

The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC PEDESTAL CONTROL

The pedestal information on both odd and even fields can be controlled on a line by line basis using the NTSC Pedestal Control Registers. This allows the pedestals to be controlled during the vertical blanking interval (lines 10 to 25).

SUBCARRIER RESET

Together with the SCRESET/RTC PIN and bits MR22 and MR21 of Mode Register 2, the ADV7177/ADV7178 can be used in subcarrier reset mode. The subcarrier will reset to field 0 at the start of the following field when a high to low transistion occurs on this input pin.

PIXEL TIMING DESCRIPTION.

The ADV7177/ADV7178 can operate in eith 8-Bit or 16-Bit YCrCb Mode.

8-Bit YCrCb Mode

This default mode accepts multiplexed YCrCb inputs through the P7-P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc. The Y, Cb and Cr data are input on a rising clock edge.

16-Bit YCrCb Mode

This mode accepts Y inputs through the P7-P0 pixel inputs and multiplexed CrCb inputs through the P15-P8 pixel inputs. The data is loaded on every second rising clock edge of CLOCK. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc.

VIDEO TIMING DESCRIPTION.

The ADV7177/ADV7178 is intended to interface to off the shelf MPEG1 and MPEG2 Decoders. As a consequence the ADV7177/ADV7178 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 Pixel Port and has several Video Timing Modes of operation that allow it to be configured as either System Master Video Timing Generator or a Slave to the System Video Timing Generator. The ADV7177/ADV7178 generates all of the required horizontal and vertical timing periods and levels for the Analog Video Outputs.

The ADV7177/ADV7178 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalisation pulses are inserted where required.

In addition the ADV7177/ADV7178 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.54MHz for NTSC and an input pixel clock of 29.5MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7177/ADV7178 has 8 distinct Master or Slave timing configurations. These are divided into 4 timing modes which operate at one discrete clock frequency (27MHz). Timing Control is establised with the bi-directional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulse widths and the where they occur in relation to each other.

Mode 0 (CCIR-656) :- Slave Option.
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7177/ADV7178 is controlled by the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the Pixel Data.

All timing Info is transmitted using a 4-byte Synchronisation Pattern. A Synchronisation pattern is sent immediately before and after each line during Active Picture and Retrace. Mode 0 is illustrated in Figure 13. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$ and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

Mode 0 (CCIR-656) :- Master Option.
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7177/ADV7178 generates H, V and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the HSYNC pin, the V bit is output on the BLANK pin and the F bit is output on the FIELD/VSYNC pin. Mode 0 is illustrated in Figure 14 (NTSC) and Figure 15 (PAL). The H V and F transitions relative to the video waveform are illustrated in Figure 16.

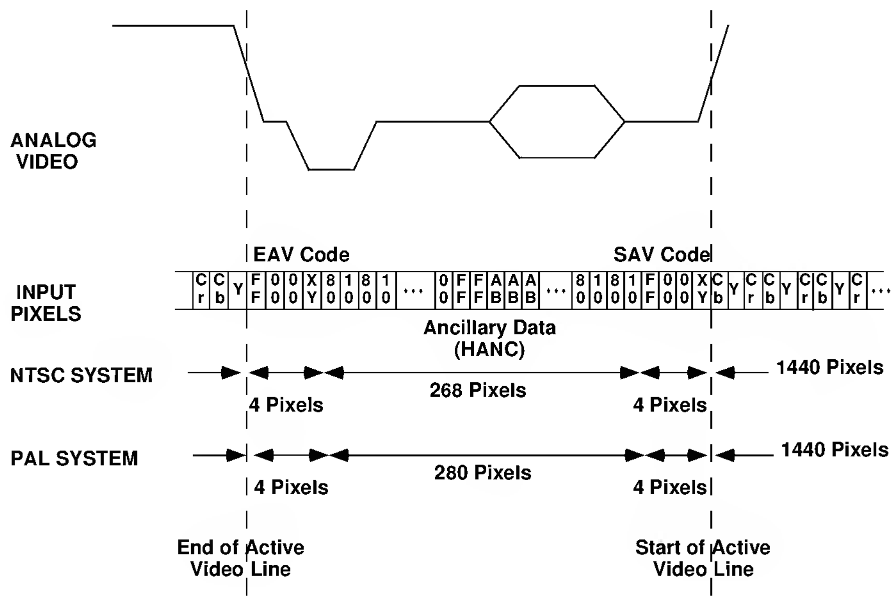


Figure 13. Timing Mode 0 (Slave Mode)

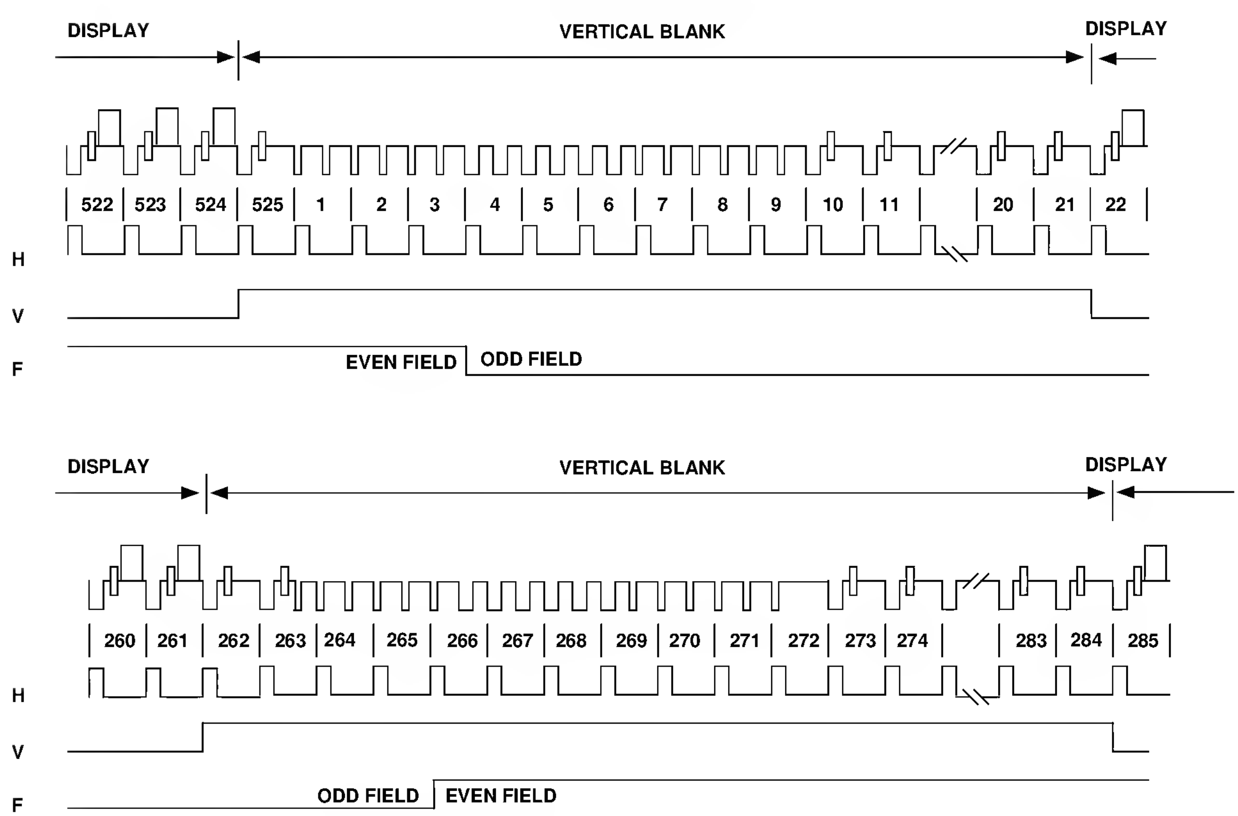


Figure 14. Timing Mode 0 (NTSC Master Mode)

Mode 1 :- Slave Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7177/ADV7178 accepts Horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7177/ADV7178 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 17 (NTSC) and Figure 18 (PAL).

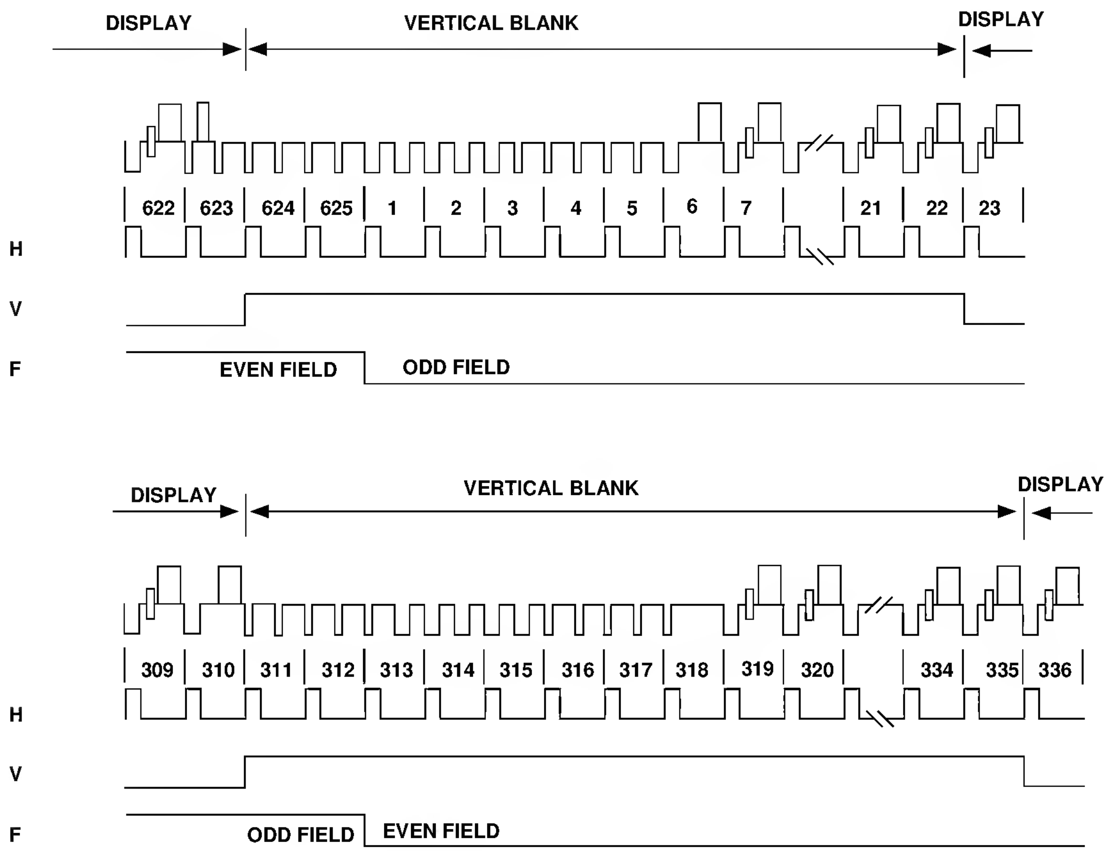


Figure 15. Timing Mode 0 (PAL Master Mode)

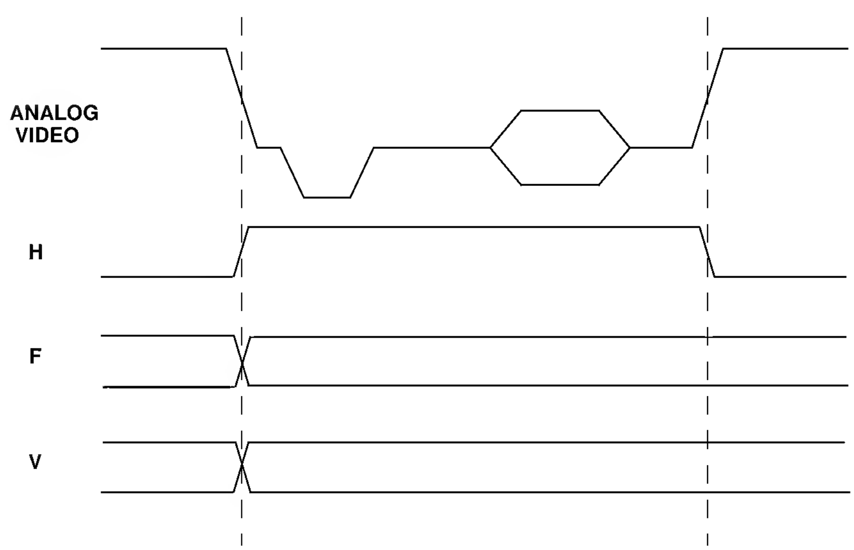


Figure 16. Timing Mode 0 Data Transitions (Master Mode)

Mode 1 :- Master Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7177/ADV7178 can generate Horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7177/ADV7178 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 17 (NTSC) and Figure 18 (PAL). Figure 19 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and FIELD for an odd or even field transition relative to the pixel data.

Mode 2 :- Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$.
(Timing Register 0 TR0 = X X X X X 1 0 0)

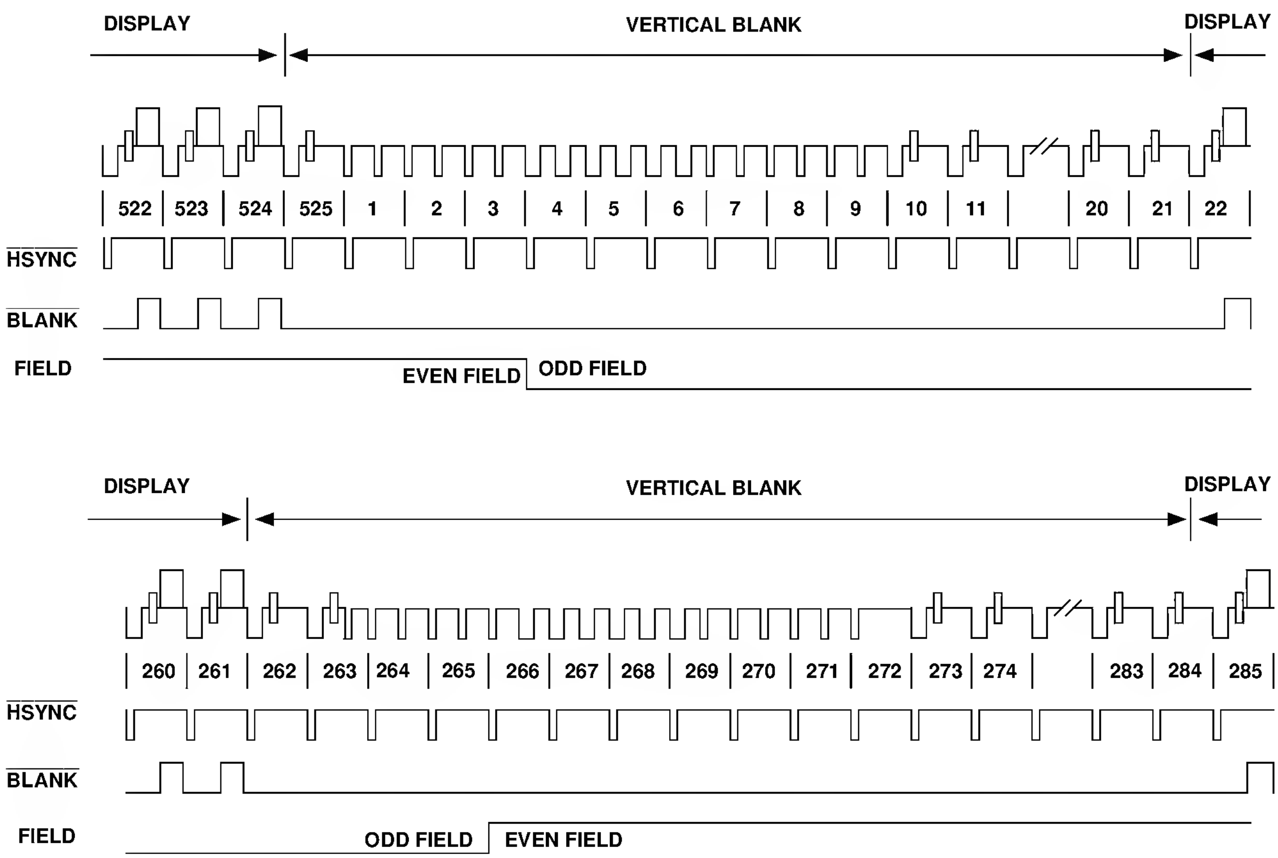


Figure 17. Timing Mode 1 (NTSC)

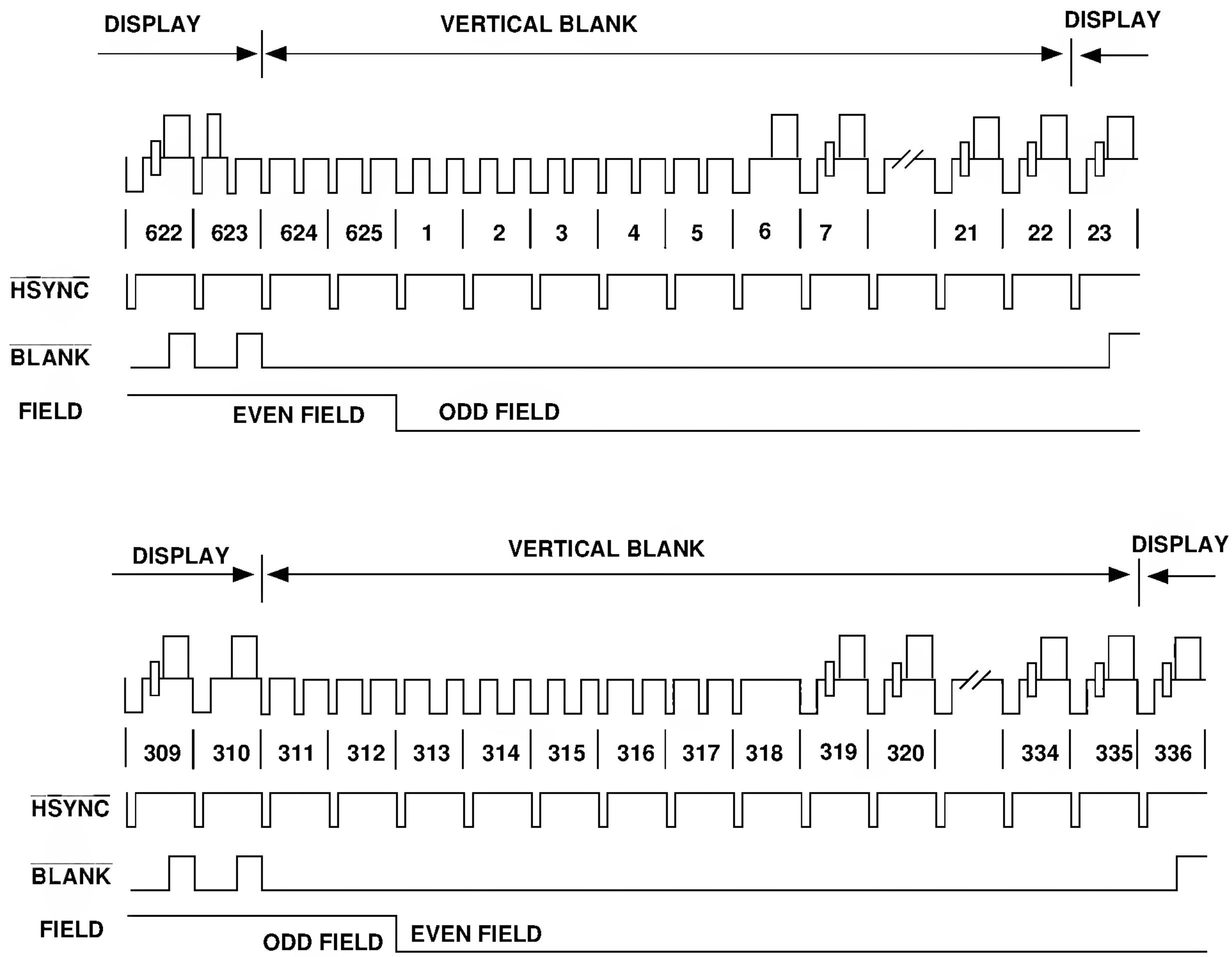


Figure 18. Timing Mode 1 (PAL)

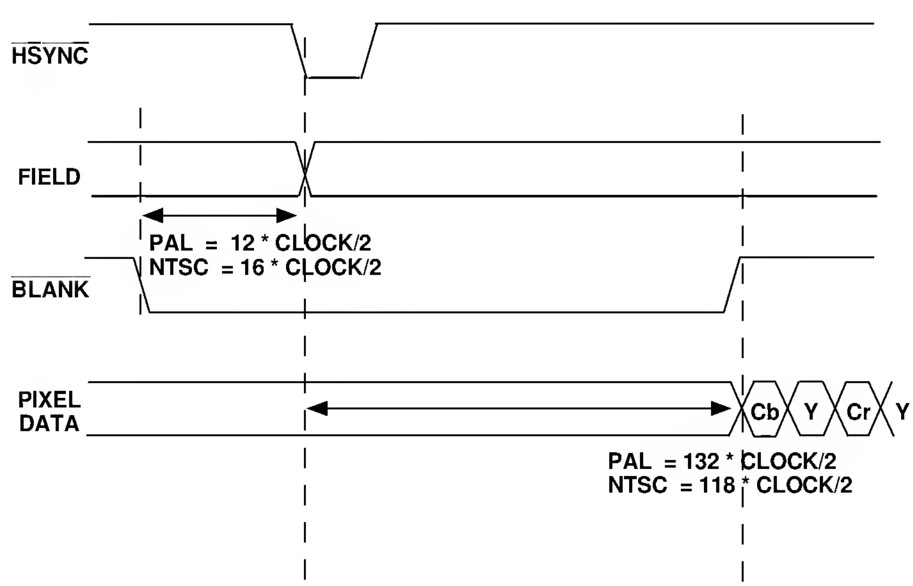


Figure 19 Timing Mode 1 Odd/Even Field Transitions

In this mode the ADV7177/ADV7178 accepts Horizontal and Vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an Odd Field. A VSYNC low transition when HSYNC is high indicates the start of an Even Field. The BLANK signal is optional. When the BLANK input is disabled the ADV7177/ADV7178 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 20 (NTSC) and Figure 21 (PAL).

Mode 2 :- Master Option HSYNC, VSYNC, BLANK.
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7177/ADV7178 can generate Horizontal and Vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an Odd Field. A VSYNC low transition when HSYNC is high indicates the start of an Even Field. The BLANK signal is optional. When the BLANK input is disabled the ADV7177/ADV7178 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 20 (NTSC) and Figure 21 (PAL). Figure 22 illustrates the HSYNC, BLANK and VSYNC for an even to odd field transition relative to the pixel data. Figure 23 illustrates the HSYNC, BLANK and VSYNC for an odd to even field transition relative to the pixel data.

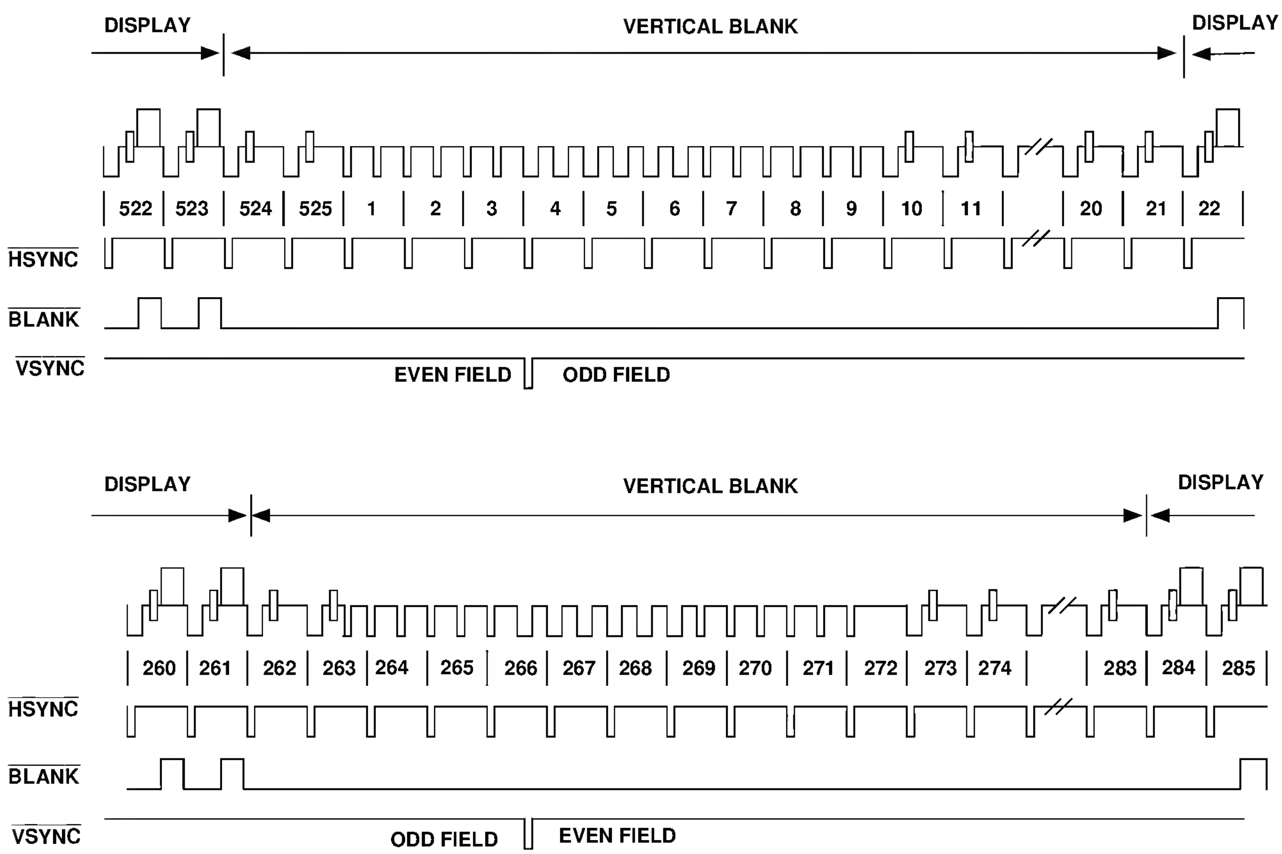
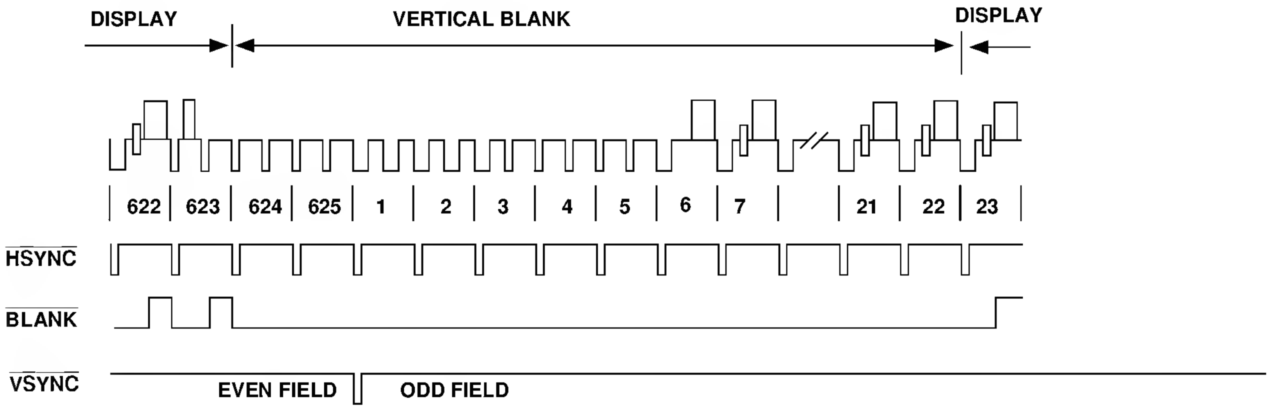


Figure 20. Timing Mode 2 (NTSC)



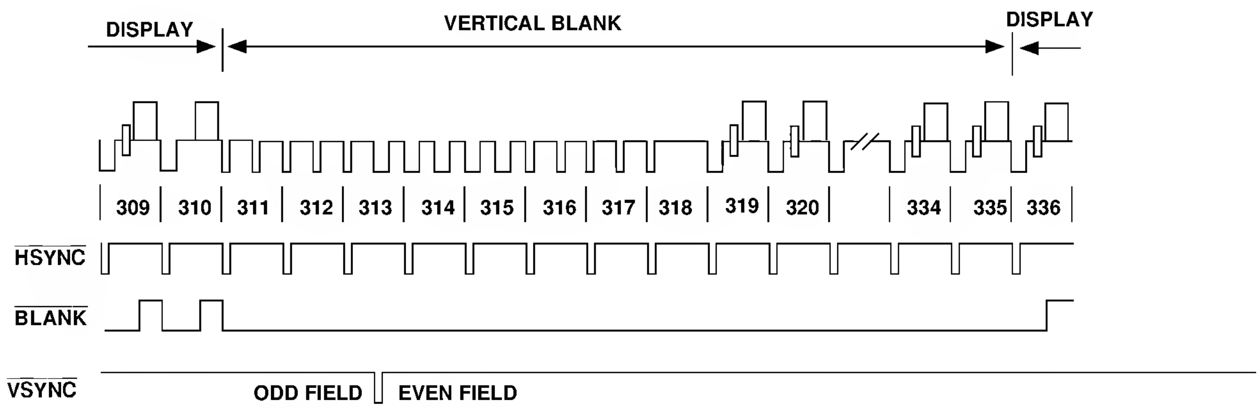


Figure 21. Timing Mode 2 (PAL)

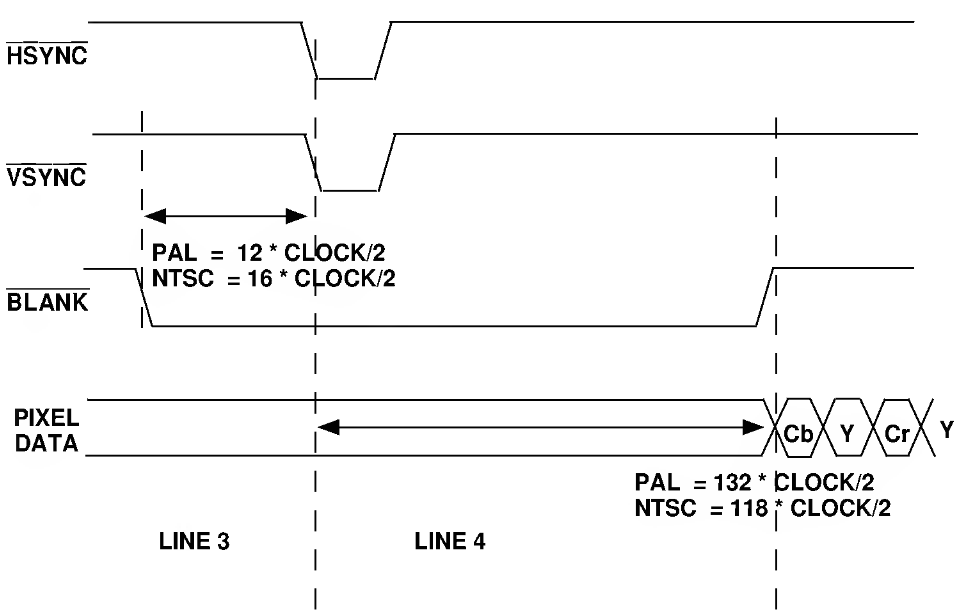


Figure 22. Timing Mode 2 Even to Odd Field Transistion

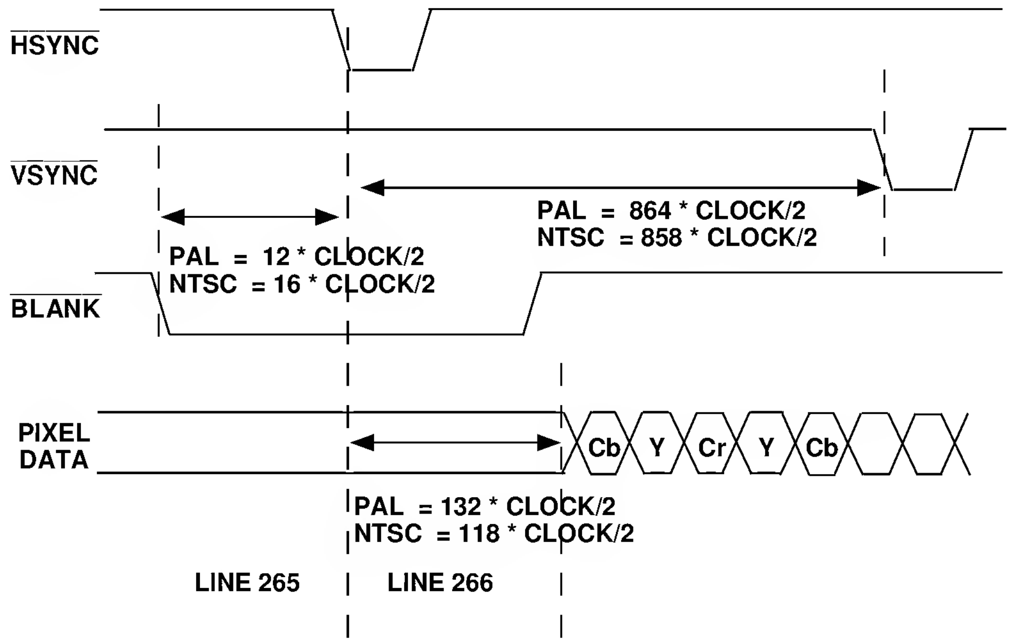


Figure 23. Timing Mode 2 Odd to Even Field Transistion

Mode 3 :- Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7177/ADV7178 accepts or generates Horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7177/ADV7178 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL).

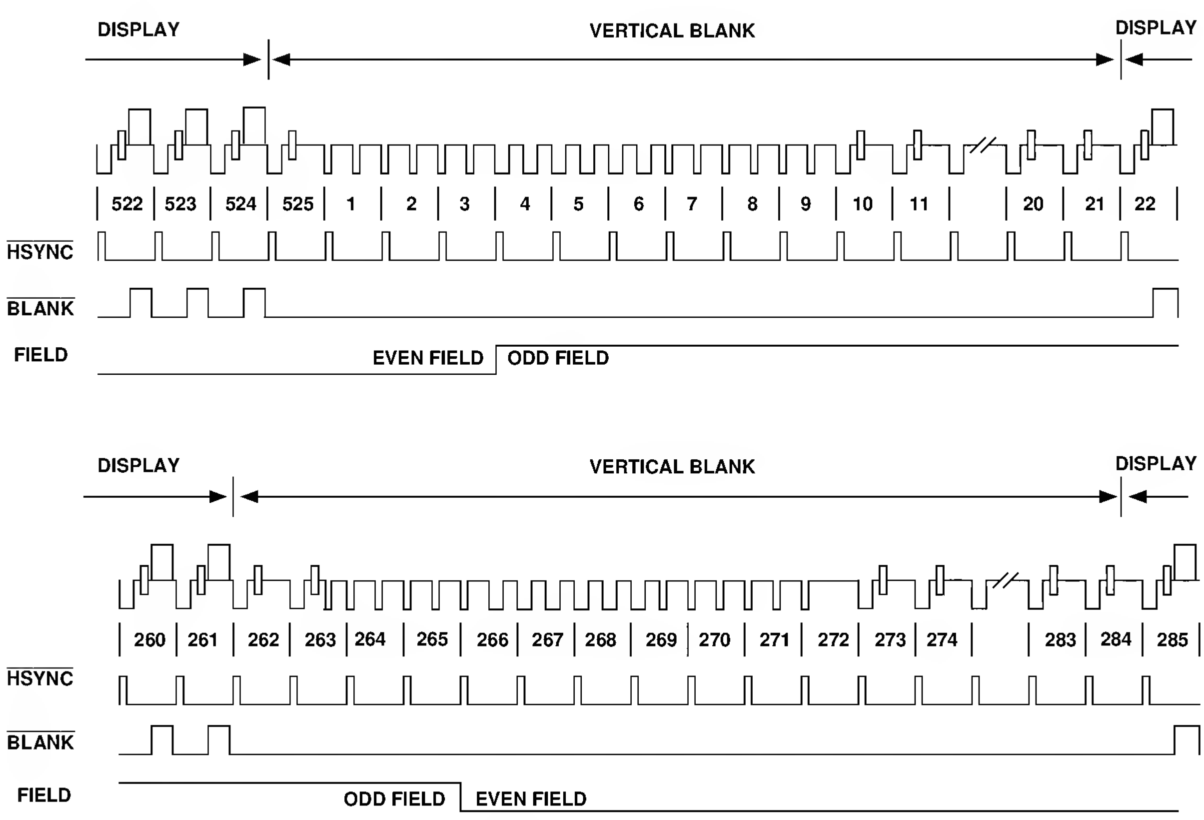


Figure 24. Timing Mode 3 (NTSC)

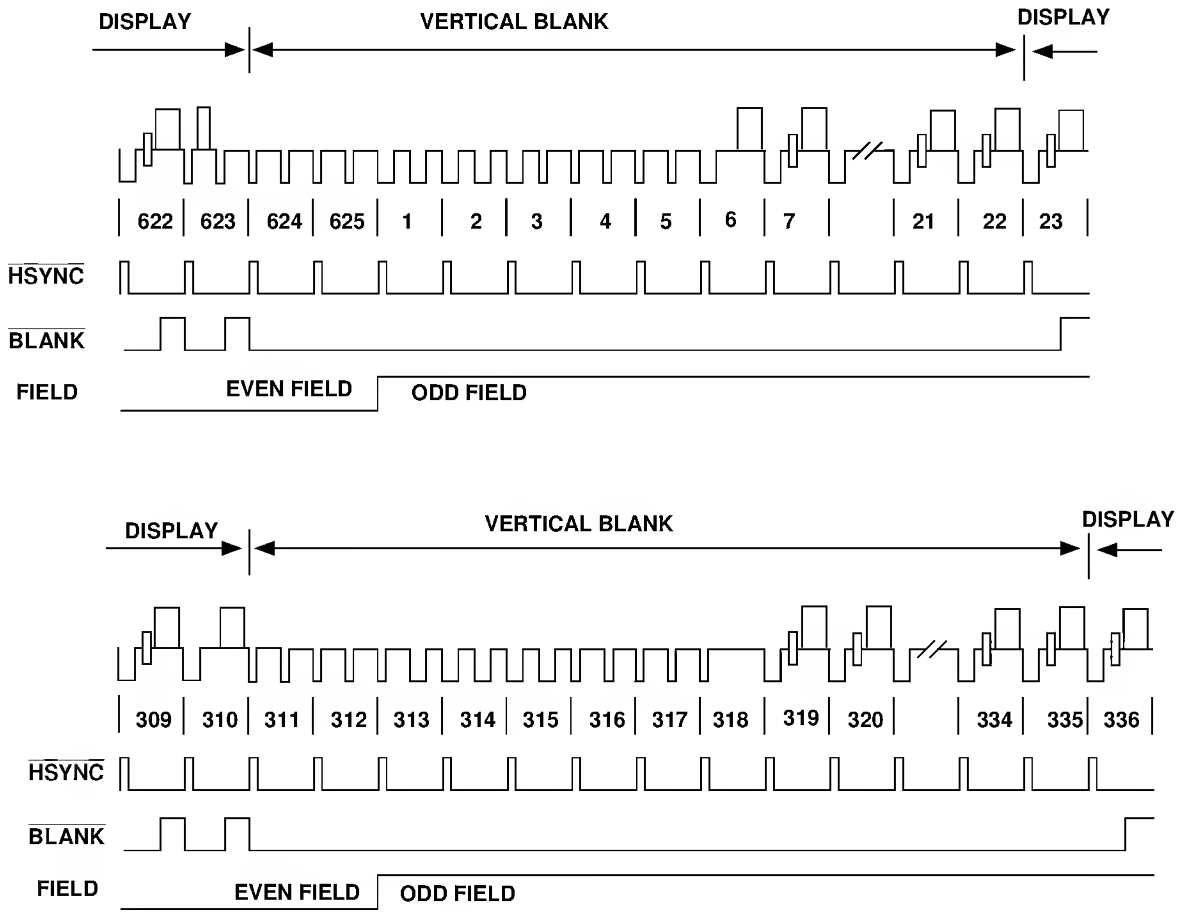


Figure 25. Timing Mode 3 (PAL)

OUTPUT VIDEO TIMING

The Video Timing Generator generates the appropriate SYNC, BLANK and BURST sequence that controls the output analog waveforms. These sequences are sumarised below. In slave modes the following sequences are synchronised with the input timing control signals. In master modes the timing generator free runs and generates the following sequences in addition to the output timing control signals.

NTSC - Interlaced :Scan Lines 1-9 and 264-272 are always blanked and vertical sync pulses are included. Scan Lines 525, 10-21 and 262, 263, 273-284 are also blanked and can be used for close captioning data. Burst is disabled on lines 1-6, 261-269 and 523-525.

NTSC- Non-Interlaced :Scan Lines 1-9 are always blanked and vertical sync pulses are included. Scan Lines 10-21 are also blanked and can be used for close captioning data. Burst is disabled on lines 1-6, 261-262.

PAL- Interlaced :Scan Lines 1-6, 311-318 and 624-625 are always blanked and vertical sync pulses are included in Fields 1, 2, 5 & 6. Scan Lines 1-5, 311-319 and 624-625 are always blanked and vertical sync pulses are included in Fields 3, 4, 7 & 8. The remaining Scan Lines in the Vertical interval are also blanked and can be used for close captionillg data. Burst is disabled on lines 1-6, 311-318 and 623-625 in Fields 1, 2, 5 & 6. Burst is disabled on lines 1-5, 311-319 and 623-625 in Fields 3, 4, 7 & 8.

PAL- Non-Interlaced :Scan Lines 1-6 and 311-312 are always blanked and veltical sync pulses are included. The remaining Scan Lines in the Vertical Interval are also blanked and can be used for close captioning data. Burst is disabled on lines 1-5, 310-312.

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high to low transistion on the $\overline{\text{RESET}}$ pin. This initializes the pixel port such that the pixel inputs P7-P0 are selected. After reset, the ADV7177/ADV7178 is automatically set up to operate in NTSC Mode. Subcarrier frequency code 21F07C16 HEX is loaded into the Sub-Carrier Frequency registers. All other registers, with the exception of Mode Register 0, are set to 00H. All bits in Mode Register 0 are set to logic level "0" except Bit MR02. Bit MR02 of Mode Register 0 is set to logic "1". This enables the 7.5IRE pedestal.

MPU PORT DESCRIPTION.

The ADV7178 and ADV7177 support a two wire serial (I^2C Compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDATA) and Serial Clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognised by a unique address. The ADV7178 and ADV7177 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 26 and Figure 27. The LSB sets either a read or write operation. Logic level "1" corresponds to a read operation while logic level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7177/ADV7178 to logic level "0" or logic level "1".

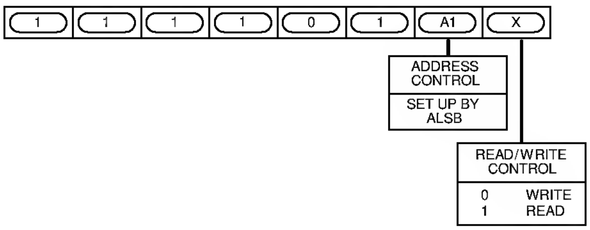


Fig 26. ADV7177 Slave Address

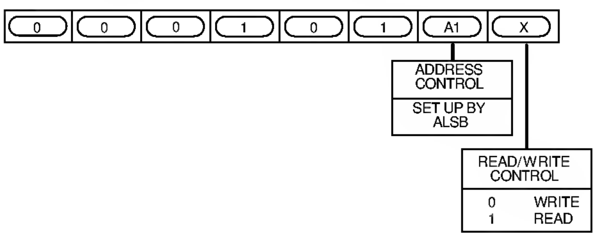


Fig 27. ADV7178 Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high to low transistion on SDATA whilst SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-Bit address + R/$\overline{W}$ bit). The bits tranferred from MSB down to LSB. The peripheral that recognises the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7177/ADV7178 acts as a standard slave device on the bus. The data on the SDATA pin is 8 bits long supporting the 7-Bit addresses plus the R/$\overline{W}$ bit. The ADV7178 has 33 subaddresses and the ADV7177 has 19 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allowing data to be written to or read from from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers. There is one exception. The Sub-Carrier Frequency Registers should be updated in sequence, starting with Sub-Carrier Frequency Register 0. The auto increment function should be then used to increment and access Sub-Carrier Frequency Registers 1, 2 and 3. The Sub-Carrier Frequency Registers should not be accessed independently.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7177/ADV7178 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.

2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7177/ADV7178 and the part will return to the idle condition.

Figure 28 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 29 shows bus write and read sequences.

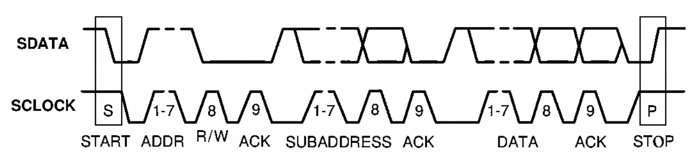


Figure 28. Write and Read Sequences

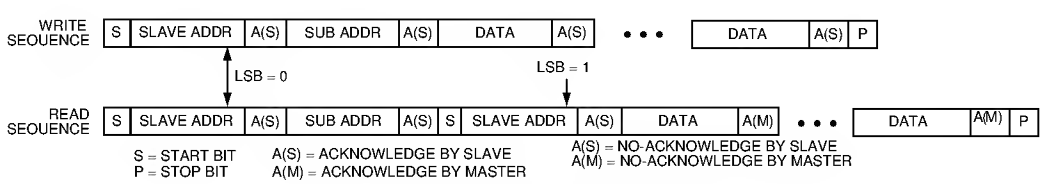


Figure 28. Bus Data Transfer

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR7-SR6 = (00)

ZERO SHOULD BE WRITTEN TO THESE BITS

ADV7178 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	SUB CARRIER FREQ REGISTER 0
0	0	0	0	1	1	SUB CARRIER FREQ REGISTER 1
0	0	0	1	0	0	SUB CARRIER FREQ REGISTER 2
0	0	0	1	0	1	SUB CARRIER FREQ REGISTER 3
0	0	0	1	1	0	SUB CARRIER PHASE REGISTER
0	0	0	1	1	1	TIMING REGISTER
0	0	1	0	0	0	Closed Captioning EXTENDED DATA - BYTE 0
0	0	1	0	0	1	Closed Captioning EXTENDED DATA - BYTE 1
0	0	1	0	1	0	Closed Captioning DATA - BYTE 0
0	0	1	0	1	1	Closed Captioning DATA - BYTE 1
0	0	1	1	0	0	TIMING REGISTER 1
0	0	1	1	0	1	MODE REGISTER 2
0	0	1	1	1	0	NTSC Pedestal CONTROL REG 0 (Field 1/3)
0	0	1	1	1	1	NTSC Pedestal CONTROL REG 1 (Field 1/3)
0	1	0	0	0	0	NTSC Pedestal CONTROL REG 2 (Field 2/4)
0	1	0	0	0	1	NTSC Pedestal CONTROL REG 3 (Field 2/4)
0	1	0	0	1	0	MODE REGISTER 3
0	1	0	0	1	1	MACROVISION REGISTER
.	.	.	.	.	.	" "
.	.	.	.	.	.	" "
1	0	0	0	1	1	MACROVISION REGISTER

ADV7177 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	SUB CARRIER FREQ REGISTER 0
0	0	0	0	1	1	SUB CARRIER FREQ REGISTER 1
0	0	0	1	0	0	SUB CARRIER FREQ REGISTER 2
0	0	0	1	0	1	SUB CARRIER FREQ REGISTER 3
0	0	0	1	1	0	SUB CARRIER PHASE REGISTER
0	0	0	1	1	1	TIMING REGISTER
0	0	1	0	0	0	Closed Captioning EXTENDED DATA- BYTE 0
0	0	1	0	0	1	Closed Captioning EXTENDED DATA- BYTE 1
0	0	1	0	1	0	Closed Captioning DATA- BYT E 0
0	0	1	0	1	1	Closed Captioning DATA- BYT E 1
0	0	1	1	0	0	TIMING REGISTER 1
0	0	1	1	0	1	MODE REGISTER 2
0	0	1	1	1	0	NTSC Pedestal CONTROL REG 0 (Field 1/3)
0	0	1	1	1	1	NTSC Pedestal CONTROL REG 1 (Field 1/3)
0	1	0	0	0	0	NTSC Pedestal CONTROL REG 2 (Field 2/4)
0	1	0	0	0	1	NTSC Pedestal CONTROL REG 3 (Field 2/4)
0	1	0	0	1	0	MODE REGISTER 3
0	1	0	0	1	1	On-Screen Display Register 0 (OSD-0)
.	.	.	.	.	.	" "
.	.	.	.	.	.	" "
0	1	1	1	1	1	On-Screen Display Register 7 (OSD-7)

Figure 30. Subaddress Register

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7177/ADV7178 except the Subaddress Register which is a write only register. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through thebus start with an access to the Subaddress Register. Then a read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register, including Subaddress Register, Mode Registers, Sub-Carrier Frequency Registers, Sub-Carrier Phase Register, Timing Registers, Closed Captioning Extended Data Registers, Closed Captioning Data Registers and NTSC Pedestal Control Registers in terms of its configuration.

Subaddress Register (SR7-SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 30 shows the various operations under the control of the Subaddress Register. Zero should always be written to SR7-SR6.

Register Select (SR5-SR0):

These bits are setup to point to the required starting address.

MR07	MR06	MR05	MR04	MR03	MR02	MR01	MR00

MR07 (0)

ZERO SHOULD BE WRITTEN TO THIS BIT

OUTPUT SELECT

MR06	
0	YC OUTPUT
1	RGB/YUV OUTPUT

MR05 (1)

"1" SHOULD BE WRITTEN TO THIS BIT

FILTER SELECT

MR04	MR03	
0	0	LOW PASS FILTER (A)
0	1	NOTCH FILTER
1	0	EXTENDED MODE
1	1	LOW PASS FILTER (B)

PEDESTAL CONTROL

MR02	
0	PEDESTAL OFF
1	PEDESTAL ON

OUTPUT VIDEO STANDARD SELECTION

MR01	MR00	
0	0	NTSC
0	1	PAL (B, D, G, H, I)
1	0	PAL (M)
1	1	RESERVED

Figure 31. Mode Register 0

MODE REGISTER 0 -MR0- (MR07-MR00)
(Address (SR4-SR0) = 00H)

Figure 31 shows the various operations under the control of Mode Register 0. This register can be read from as well written to.

-MR0 BIT DESCRIPTION-

Encode Mode Control (MR01-MR00):
These bits are used to setup the encode mode. The ADV7177/ADV7178 can be set up to output NTSC, PAL (B,D,G,H,I), PAL(M) and PAL(N) standard video.

Pedestal Control (MR02):
This bit specifies whether a pedestal is to be generated on the NTSC composite video signal. This bit is invalid if the ADV7177/ADV7178 is configured in PAL mode.

Luminance Filter Control (MR04-MR03):
These bits are used for selecting between a filter for the luminance signal. These filters automatically are set to the cutoff frequency for the Low Pass Filters and the sub-carrier frequency for the Notch Filter. The extended mode filter is a 5.5MHz low pass filter. The filters are illustrated in Figures 3 to 11.

MR05:
This bit must alwats be set to logical "1"

Output Control (MR06):
This bit specifies if the part is in composite video or RGB/YUV mode. Please note that in RGB/YUV mode the main composite signal is still available.

MODE REGISTER 1 MR1 (MR17-MR10)
(Address (SR4-SR0) = 01H)

Figure 32 shows the various operations under the control of Mode Register 1. This register can be read from as well written to.

-MR1 BIT DESCRIPTION-

Interlaced Mode Control (MR10):
This bit is used to setup the output to interlaced or non-interlaced mode. This mode is only relevant when the part is in composite video mode.

Closed Captioning Field Control (MR12-MR11)
These bits control the field that close captioning data is displayed on close captioning information can be displayed on an odd field, even field or both fields.

DAC Control (MR16-MR13):
These bits can be used to power down the DACs. This can be used to reduce the power consumption of the ADV7177/ADV7178 if any of the DACs are not required in the application.

Color Bar Control (MR17):
This bit can be used to generate and output an internal color bar. The color bar configuration is 75/7.5/75/7.5 for NTSC and 100/0/75/0 for PAL.

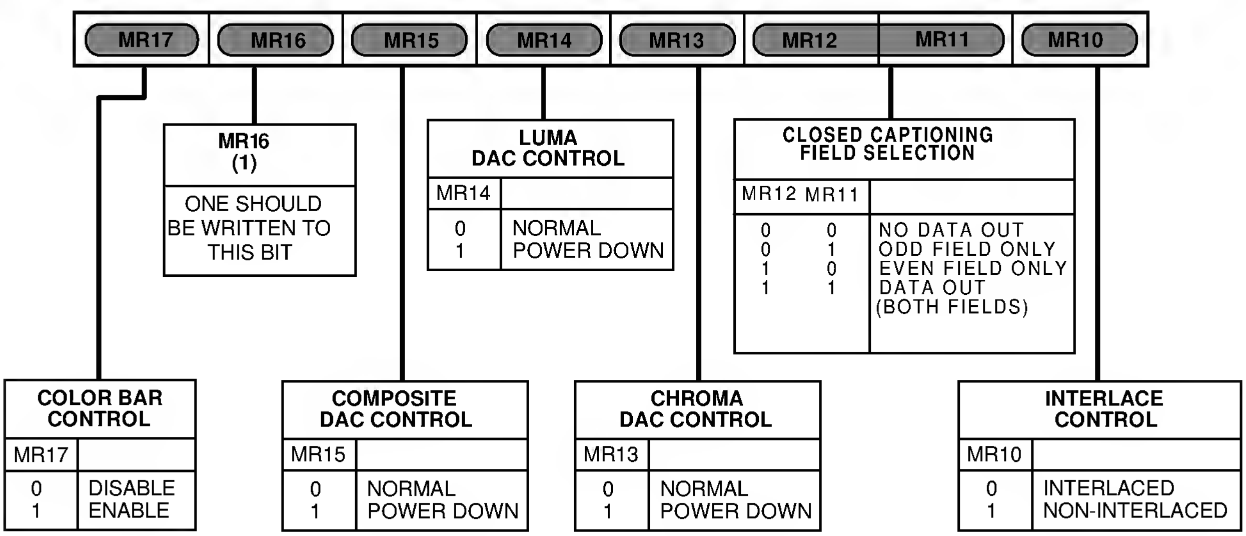


Figure 32. Mode Register 1

COLOR SUB-CARRIER FREQUENCY REGISTERS 3-0 (FSC3-FSC0)

(Address (SR4-SR0) = 05H-02H)

These 8-Bit wide registers are used to set up the Sub-Carrier Frequency. The value of these registers are calculated by using the following equation:

$$\text{Sub-Carrier Frequency Register} = \frac{2^{32} - 1}{F_{CLK}} * F_{SCF}$$

i.e.: NTSC Mode,
F_{CLK} = 27 MHz,
F_{SCF} = 3.5796 54 MHz

$$\text{Sub-Carrier Freq Value} = \frac{(2^{32} - 1) * 3.57954 \times 10^6}{27 \times 10^6}$$

$$= \text{21F07C16 HEX}$$

Figure 33 shows how the frequency is set up by the 4 registers

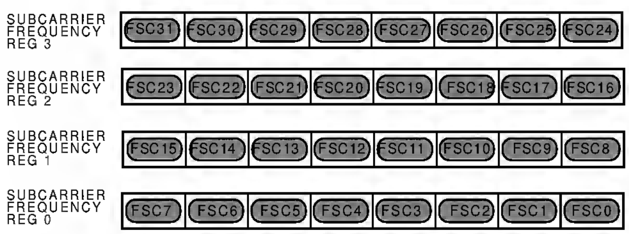


Figure 33. Sub Carrier Frequency Register

SUB-CARRIER PHASE REGISTER (FP7-FP0):

(Address (SR4-SR0) = 06H)

This 8-Bit wide register is used to set up the Sub-Carrier Phase. Each bit represents 1.41°.

TIMING REGISTER 0 (TR07-TR00)

(Address (SR4-SR0) = 07H)

Figure 34 shows the various operations under the control of Timing Register 0. This register can be read from as well written to.

- TR0 BIT DESCRIPTION-

Master/Slave Control (TR00):
This bit controls whether the ADV7177/ADV7178 is in master or slave mode.

Timing Mode Control (TR02-TR01):
These bits control the timing mode of the ADV7177/ADV7178. These modes are described in the Timing and Control section of the datasheet.

$\overline{\text{BLANK}}$ Control (TR03):
This bit controls whether the $\overline{\text{BLANK}}$ input is used when the part is in slave mode.

Luma Delay Control (TR05-TR04):
These bits control the addition of a luminance delay. Each bit represents a delay of 74ns.

Pixel Port Select (TR06):
This bit is used to set the pixel port to accept 8-Bit or 16-Bit data. If an 8-Bit input is selected the data will be set up on pins P7-P0.

Timing Register Reset (TR07):
Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after setting up a new timing mode.

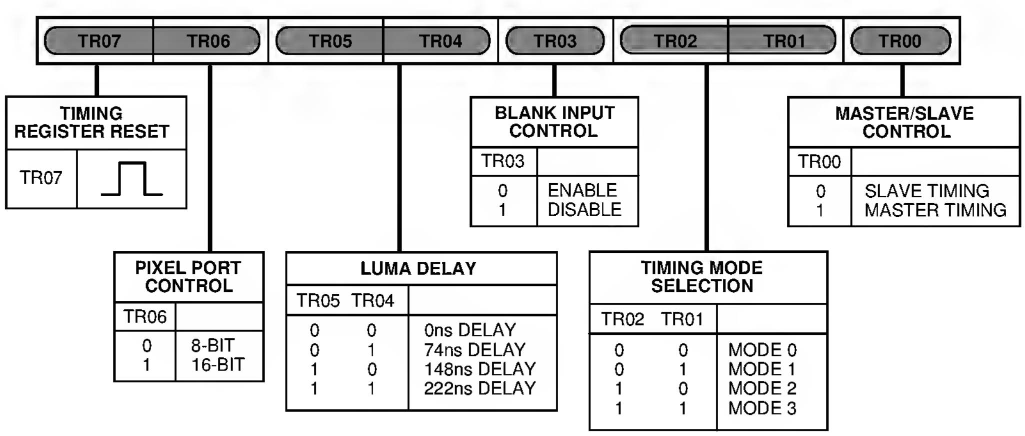


Figure 34. Timing Register 0

CLOSED CAPTIONING EXTENDED DATA REGISTER 1-0 (CED15-CED00) (Address (SR4-SR0) = 09-08H)

These 8-Bit wide registers are used to set up the closed captioning extended data bytes. Figure 35 shows how the high and low bytes are set up in the registers.

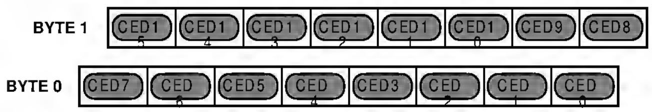


Figure 35. Closed Captioning Extended Data Register

CLOSED CAPTIONING DATA REGISTER 1-0 (CCD15-CCD00) (Subaddress (SR4-SR0) = 0B-0AH)

These 8-Bit wide registers are used to set up the closed captioning data bytes. Figure 36 shows how the high and low bytes are set up in the registers.

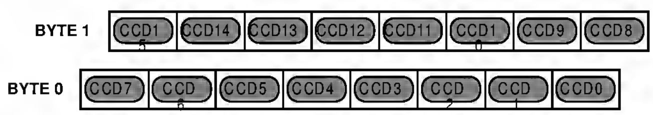


Figure 36. Closed Captioning Data Register

TIMING REGISTER 1 (TR17-TR10) (Address (SR4-SR0) = 0CH)

Timing Register 1 is an 8-Bit wide register.

Figure 37 shows the various operations under the control of Timing Register 1. This register can be read from as well written to. This register can be used to adjust the width and position of the master mode timing signals.

-TR1 BIT DESCRIPTION-

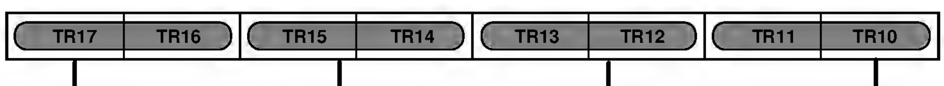
$\overline{\text{HSYNC}}$ Width (TR11-TR10):
These bits adjust the $\overline{\text{HSYNC}}$ pulse width.

$\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$/FIELD Delay Control (TR13-TR12):
These bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD/$\overline{\text{VSYNC}}$ output.

$\overline{\text{HSYNC}}$ to FIELD Delay Control (TR15-TR14):
When the ADV7177/ADV7178 is in timing mode 1, these bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD output rising edge.

$\overline{\text{VSYNC}}$ Width (TR15-TR14):
When the ADV7177/ADV7178 is in timing mode 2, these bits adjust the $\overline{\text{VSYNC}}$ pulse width.

$\overline{\text{HSYNC}}$ to Pixel Data Adjust (TR17-TR16):
This enables the $\overline{\text{HSYNC}}$ to be adjusted with respect to the pixel data. This allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.



HSYNC TO PIXEL DATA ADJUSTMENT

TR17	TR16	
0	0	0 x T_{PCLK}
0	1	1 x T_{PCLK}
1	0	2 x T_{PCLK}
1	1	3 x T_{PCLK}

HSYNC TO FIELD RISING EDGE DELAY (MODE 1 ONLY)

TR15	TR14	T_c
x	0	T_b
x	1	T_b + 32µs

VSYNC WIDTH (MODE 2 ONLY)

TR15	TR14	
0	0	1 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	128 x T_{PCLK}

HSYNC TO FIELD/VSYNC DELAY

TR13	TR12	T_b
0	0	1 x T_{PCLK}
0	1	3 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	64 x T_{PCLK}

HSYNC WIDTH

TR11	TR10	T_a
0	0	1 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	128 x T_{PCLK}

TIMING MODE 1 (MASTER/PAL)

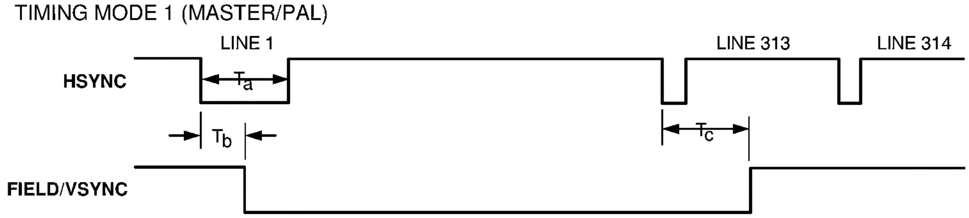


Figure 37. Timing Register 1

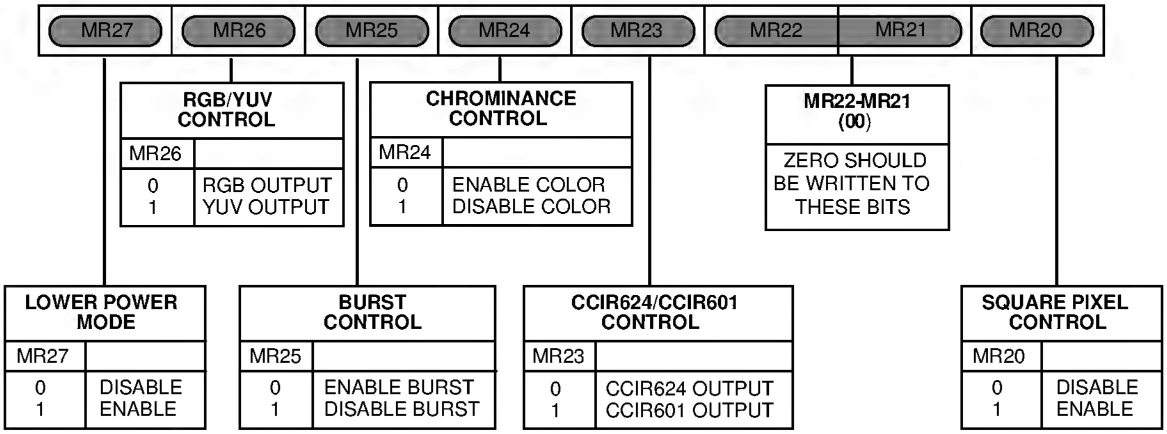


Figure 38. Mode Register 2

MODE REGISTER 2 MR2 (MR27-MR20)
(Address (SR4-SR0) = 0DH)

Mode Register 2 is a 8-Bit wide register.

Figure 38 shows the various operations under the control of Mode Register 2. This register can be read from as well written to.

- MR2 BIT DESCRIPTION-

Square Pixel Mode Control (MR20):
This bit is used to setup square pixel mode. This is available in slave mode only. For NTSC, a 24.54MHz clock must be supplied. For PAL, a 29.5MHz clock must be supplied.

MR22-MR21
These bits should be written with zeroes

CCIR624/CCIR601 Control (MR23)
This bit switches the video output between CCIR624 and CCIR601 video standard.

Chrominance Control (MR24)
This bit enables the color information to be switched on and off the video output.

Burst Control (MR25)
This bit enables the burst information to be switched on and off the video output.

RGB/YUV Control (MR26)
This bit enables the output from the RGB DACs to be set to YUV output video standard. Bit MR06 of Mode Register 0 must be set to logic level "1" before MR26 is set.

Lower Power Control (MR27)
This bit enables the lower power operational mode of the ADV7177/ADV7178.

NTSC PEDESTAL CONTROL REGISTERS 3-0 (PCE15-0, PCO15-0)

(Subaddress (SR4-SR0) = 11-0EH)
These 8-Bit wide registers are used to set up the NTSC pedestal on a line by line basis in the vertical blanking interval for both odd and even fields. Figure 39 shows the four control registers. A logic "1" in any of the bits of these registers has the effect of turning the pedestal off on the equivalent line.

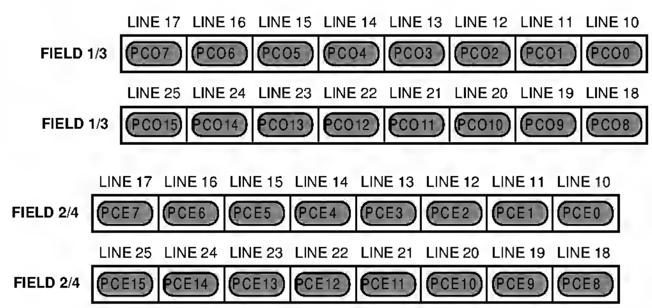


Figure 39. Pedestal Control Registers

MODE REGISTER 3 MR3 (MR37-MR30) (Address (SR4-SR0) = 12H)

Mode Register 3 is a 8-Bit wide register.

Figure 34 shows the various operations under the control of Mode Register 3. Bits MR36-MR30 are reserved and logic "0" should be written to them.

-MR3 BIT DESCRIPTION-

DAC Switching Control (MR37):
This bit is used to switch the luminance signal onto the composite DAC. Figure 40 illustrates the DAC outputs and how they switch when MR37 is set to logic "1".

Revision Code (MR30):
This bit is read only and indicates the revision of the device.

VBI Passthrough Control (MR31):
This bit determines whether or not data in the Vertical Blanking Interval (VBI) is output to the analog outputs or blanked.

Master CLOCK Control (MR33-MR32):
These bits contol the CLOCK Out (13.5 MHz) status. This output, which can be used to drive external devices (eg MPEG Decoder) can be enabled/disabled and set to either 27 MHz or 13.5 MHz.

Input Default Color (MR36):
This bit determines the default output color from the DACs for zero input data (or disconnected). A logical "0" means that the color corresponding to 00000000 will be displayed. A logical "1" forces the output color to black for 00000000 input video data.

DAC Output Selection/Switching:
This bit determines which video output format is assigned to each of the three DACs.

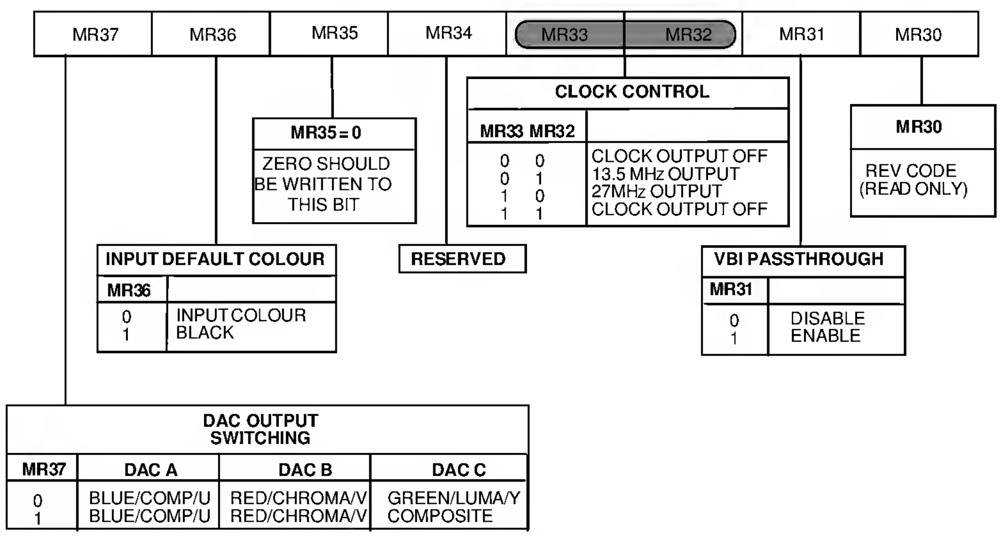


Figure 40. Mode Register 3

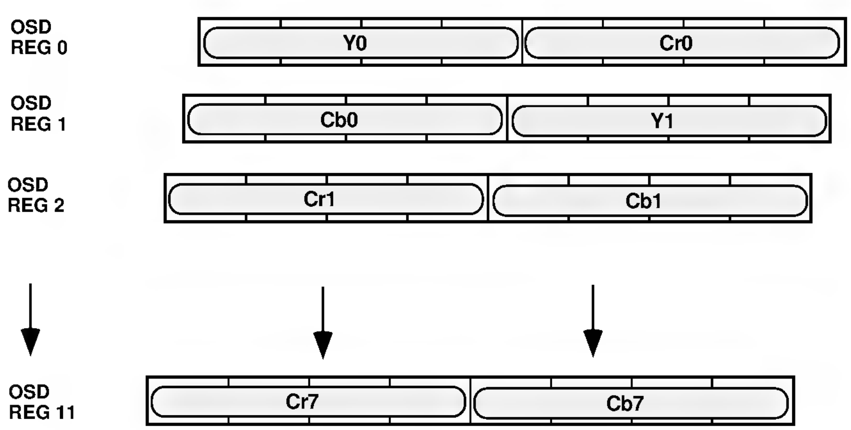


Figure 41. OSD Registers

APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7177/ADV7178 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7177/ADV7178 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7177/ ADV7178 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7177/ADV7178, the analog output traces, and all the digital signal traces leading up to the ADV7177/ADV7178. The ground plane is the board's common ground plane.

Power Planes

The ADV7177/ADV7178 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7177/ADV7178.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7177/ADV7178 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7177/ ADV7178 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7177/ADV7178 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7177/ADV7178 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7177/ADV7178 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

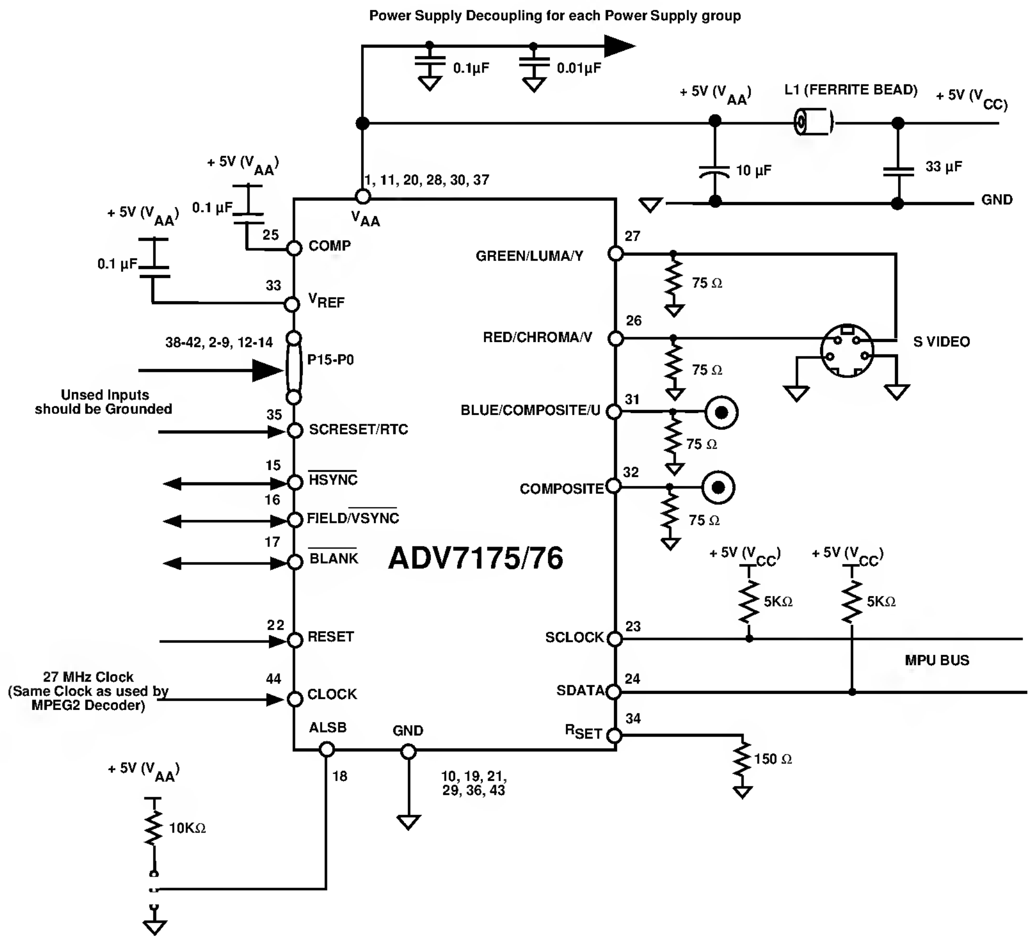
The ADV7177/ADV7178 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Inputs, especially Pixel Data Inputs and clocking signals should never overlay any of the analog signal circuitry and should be kept as far away as possible.

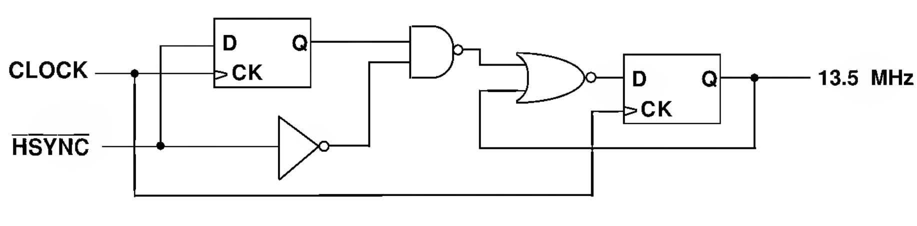
For best performance, the outputs should each have a 75 ý load resistor connected to GND. These resistors should be placed as close as possible to the ADV7177/ADV7178 so as to minimize reflections.

The ADV7177/ADV7178 should have no inputs left floating. Any inputs that are not required should be tied to ground.



Recommended Analog Circuit Layout

The circuit below can be used to generate a 13.5 MHz waveform using the 27 MHz clock and the $\overline{\text{HSYNC}}$ pulse. This waveform is guaranteed to produce the 13.5 MHz clock in synchronization with the 27 MHz clock. This 13.5 MHz clock can be used if 13.5 MHz clock is required by the MPEG decoder. This will guarantee that the Cr and Cb pixel information is input to the ADV7177/ADV7178 in the correct sequence.



Circuit to generate 13.5 MHz

APPENDIX 2

CLOSED CAPTIONING

The ADV7177/ADV7178 supports closed captioning conforming to the standard Television Synchronizing Waveform for Color Transmission. Closed captioning is transmitted during the blanked active line time of line 21 of the odd fields.

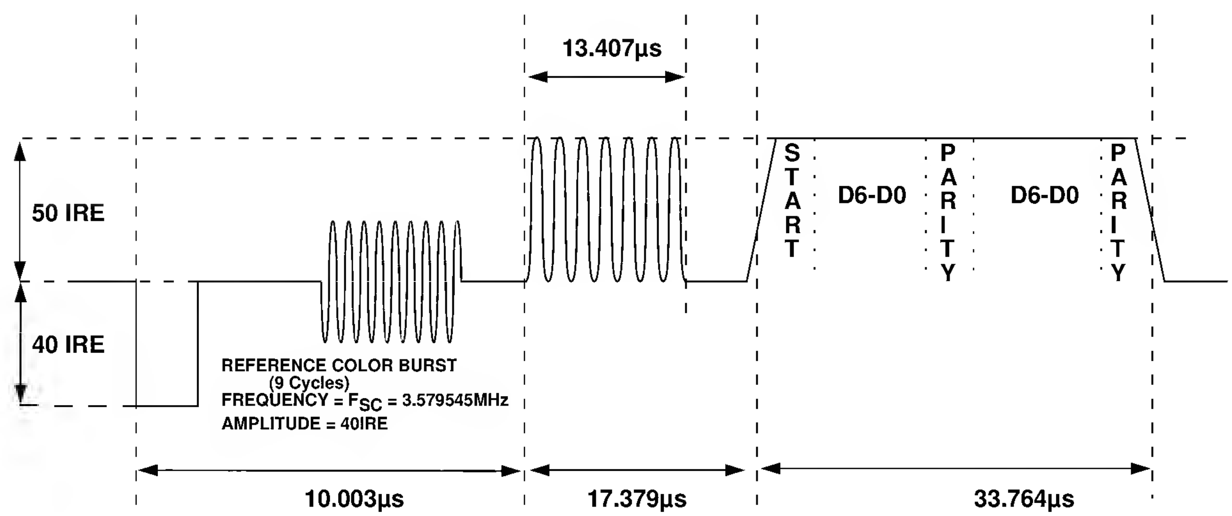
Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run in signal, the blanking level is held for two data bits and is followed by a logic level "1" start bit.

16 bits of data follow the start bit. These consist of two 8-Bit bytes. The data for these bytes is stored in Closed Captioning Data Registers 0 and 1.

The ADV7177/ADV7178 also supports the extended closed captioning operation which is active during even fields and is encoded on scan line 284. The data for this operation is stored in Closed Captioning Extended Data Registers 0 and 1.

All clock run-in signals and timing to support Closed Captioning on lines 21 and 282 are generated automatically by the ADV7177/ADV7178. All pixels inputs are ignored during lines 21 and 282.

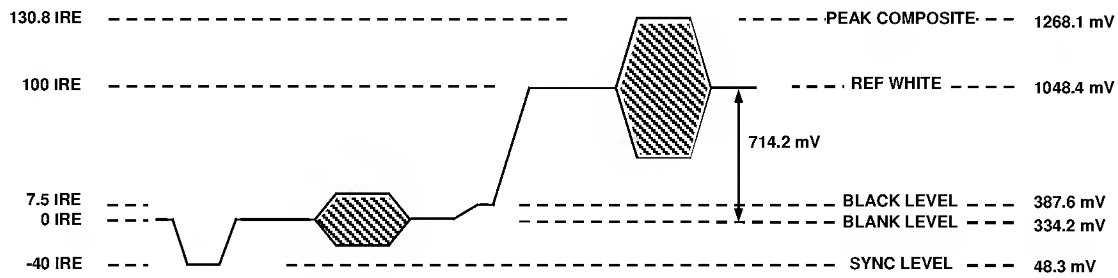
FCC Code of Federal Regulations (CFR) 47 section 15.119 and EIA208 describe the closed captioning information for lines 21 and 284.



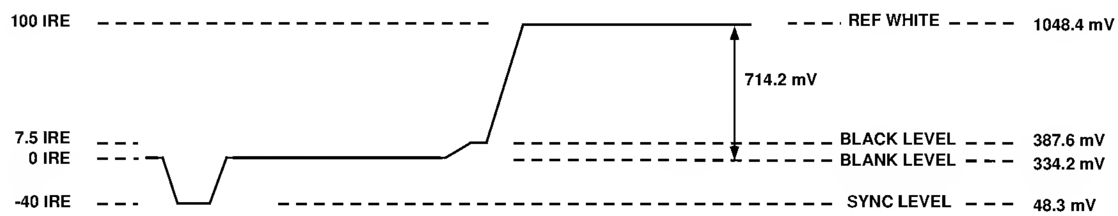
Closed Captioning Waveform (NTSC)

APPENDIX 3

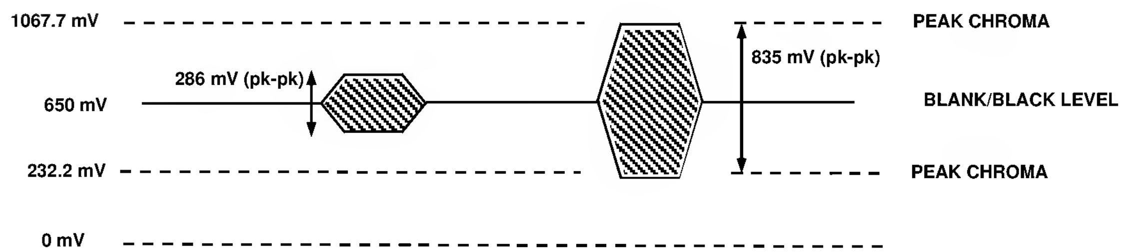
NTSC WAVEFORMS (WITH PEDESTAL)



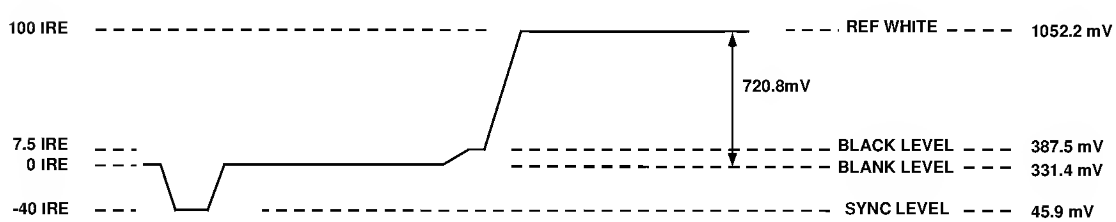
NTSC Composite Video Levels



NTSC Luma Video Levels

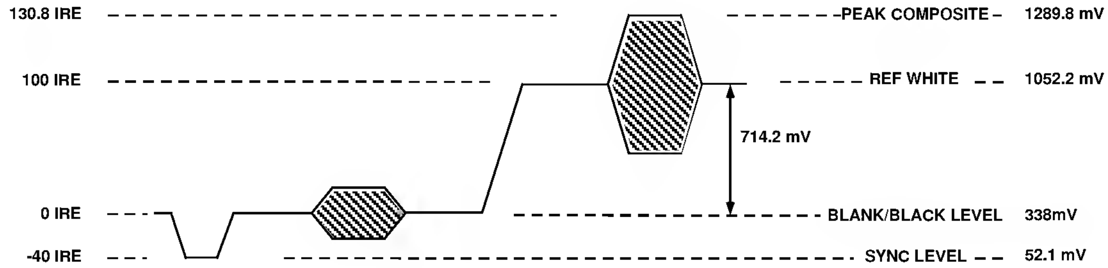


NTSC Chroma Video Levels

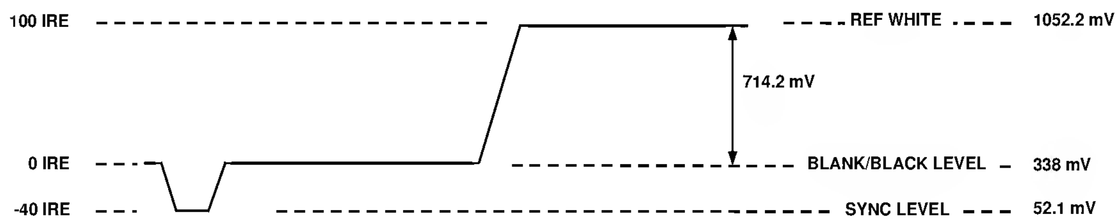


NTSC RGB Video Levels

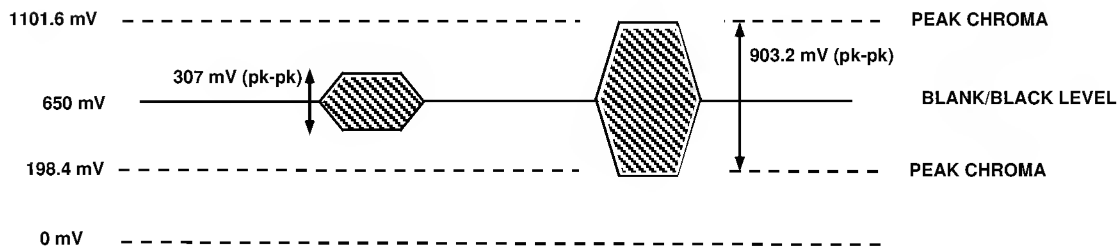
NTSC WAVEFORMS (WITHOUT PEDESTAL)



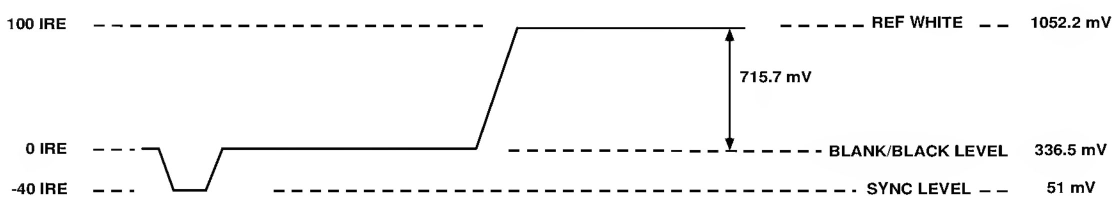
NTSC Composite Video Levels



NTSC Luma Video Levels

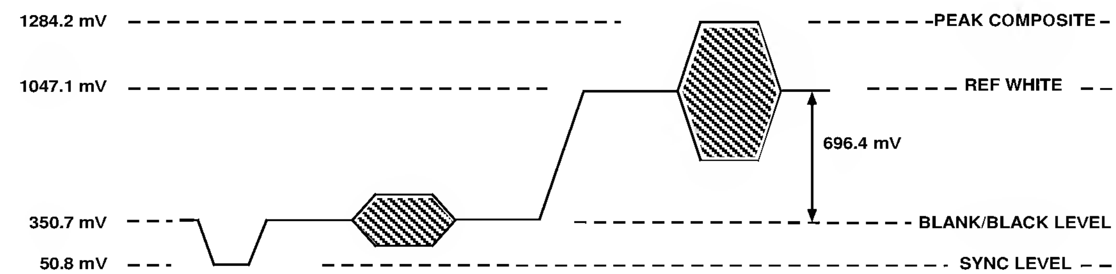


NTSC Chroma Video Levels

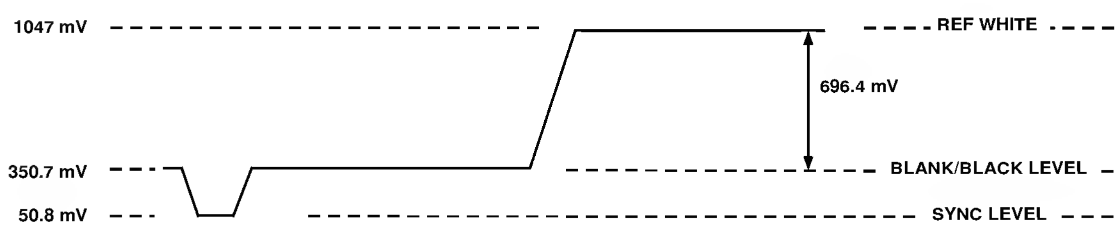


NTSC RGB Video Levels

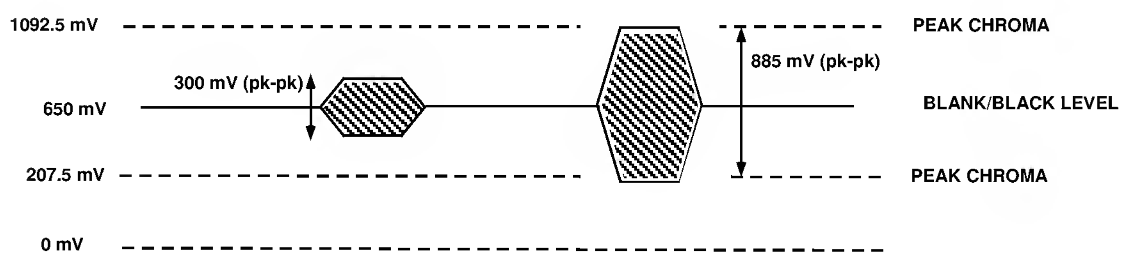
PAL WAVEFORMS



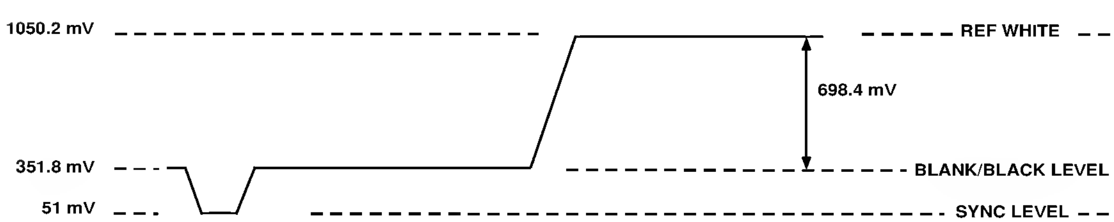
PAL Composite Video Levels



PAL Luma Video Levels



PAL Chroma Video Levels



PAL RGB Video Levels

APPENDIX 4
REGISTER VALUES

The ADV7177/ADV7178 registers can be set depending on the user standard required.

The following examples give the various register formats for several video standards.

In each case the output is set to composite o/p with all DACs powered up and with the $\overline{\text{BLANK}}$ input control disabled. Additionally, the burst and color information are enabled on the output and the internal color bar generator is switched off. In the examples shown the timing mode is set to Mode 0 in slave format. TR02-TR00 of the Timing Register 0 control the timing modes. For a detailed explanation of each bit in the command registers, please turn to the Register Programming section of the datasheet. TR07 should be toggled after setting up a new timing mode. Timing Register 1 provides additional control over the position and duration of the timing signals. In the examples this register is programmed in default mode.

NTSC

Mode Register 0	04 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	16 Hex
Subcarrier Frequency Register 1	7C Hex
Subcarrier Frequency Register 2	F0 Hex
Subcarrier Frequency Register 3	21 Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

PAL (B, D, G, H, I)

Mode Register 0	01 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	CB Hex
Subcarrier Frequency Register 1	8A Hex
Subcarrier Frequency Register 2	09 Hex
Subcarrier Frequency Register 3	2A Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

PAL (M)

Mode Register 0	06 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	A3 Hex
Subcarrier Frequency Register 1	EF Hex
Subcarrier Frequency Register 2	E6 Hex
Subcarrier Frequency Register 3	21 Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

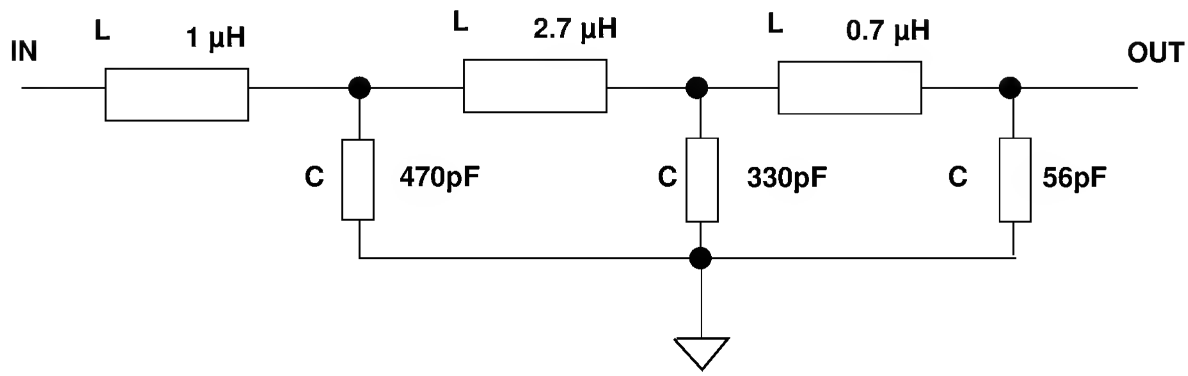
PAL (N)

Mode Register 0	05 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	CB Hex
Subcarrier Frequency Register 1	8A Hex
Subcarrier Frequency Register 2	09 Hex
Subcarrier Frequency Register 3	2A Hex

APPENDIX 5

OUTPUT FILTER

If an output filter is required for the composite output of the ADV7177/ADV7178, The following filter can be used. Plots of the filter characteristics can be produced on request.



APPENDIX 6

OUTPUT WAVEFORMS

100/75% Color Bars NTSC

100/75% Color Bars PAL

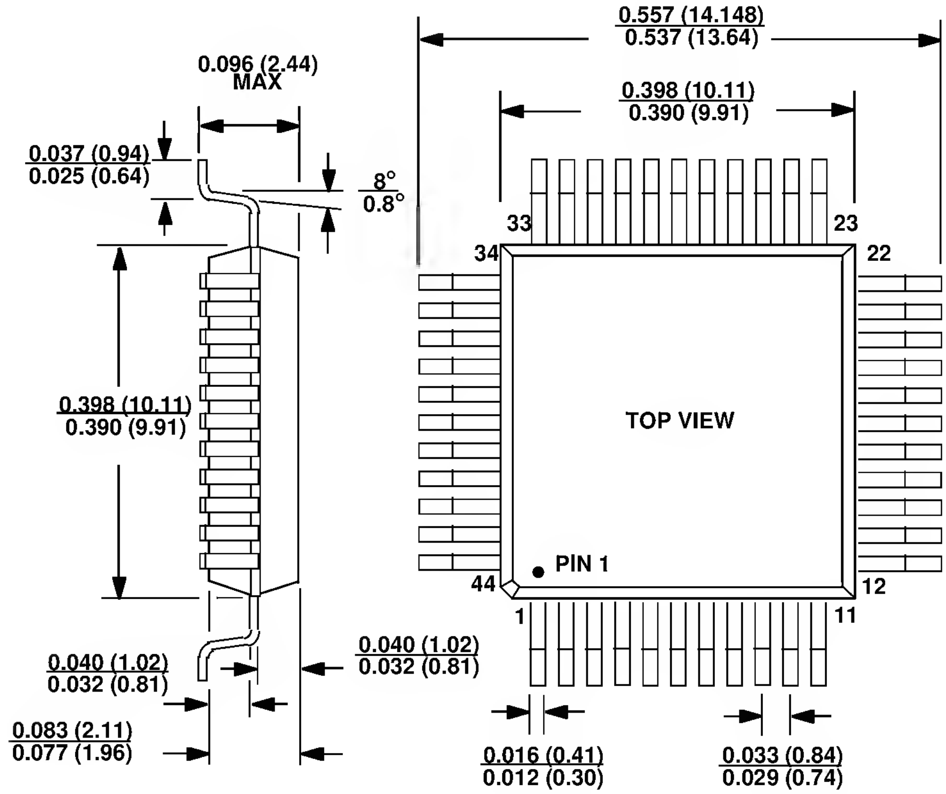
Differential Phase and Gain Measurements (PAL)

Vectorscope Measurements (PAL)

Modulated Ramp Measurements (PAL)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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